200-mA LOW-I_Q LOW-DROPOUT REGULATOR FOR PORTABLE DEVICES

Check for Samples: TLV70012A-Q1, TLV70025-Q1, TLV70028-Q1, TLV70030-Q1, TLV70032-Q1, TLV70033-Q1

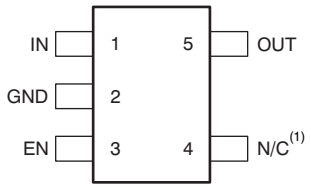
FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C4B**
- **2% Accuracy**
- **Low I_Q: 31 µA**
- **Fixed Output Voltage of 3.3 V**
- **High PSRR: 68 dB at 1 kHz**
- **Stable With Effective Capacitance of 0.1 µF**
- **Thermal Shutdown and Overcurrent Protection**
- **Latch-Up Performance Meets 100 mA Per AEC-Q100, Level I**
- **Available in the SOT23-5 (DDC) and SC70-5 (DCK) Packages**

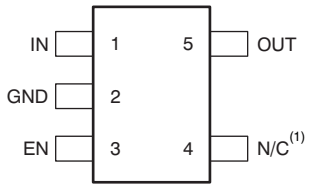
APPLICATIONS

Automotive

TLV700xx-Q1 DDC SOT23-5 PACKAGE (TOP VIEW)



TLV700xx-Q1 DCK SC70-5 PACKAGE (TOP VIEW)

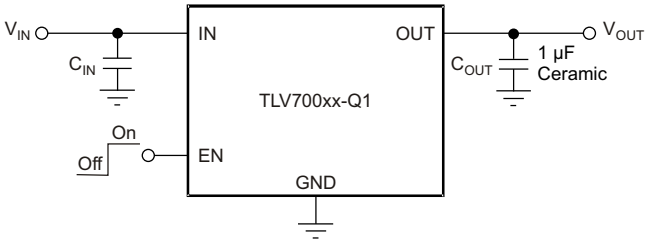


DESCRIPTION

The TLV700xx-Q1 family of low-dropout (LDO) linear regulators are low-quiescent-current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision band-gap and error amplifier provides overall 2% accuracy. Low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage make this series of devices ideal for most battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

The TLV700xx-Q1 LDOs are available in the SOT23-5 (DDC) and the SC70-5 (DCK) packages.



Typical Application Circuit (Fixed-Voltage Versions)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

At T_A = –40°C to 125°C (unless otherwise noted). All voltages are with respect to GND.

V_{IN}	Input voltage range		–0.3 V to 6 V
V_{EN}	Enable voltage range		–0.3 V to 6 V
V_{OUT}	Output voltage range		–0.3 V to 6 V
I_{OUT}	Maximum output current		Internally limited
	Output short-circuit duration		Indefinite
T_A	Operating ambient temperature range		–40°C to 125°C
T_{stg}	Storage temperature range		–55°C to 150°C
	Electrostatic discharge rating	Human body model (HBM) H2	2 kV
		Charged device model (CDM) C4B	750 V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV700xx-Q1 DCK (5 PINS)	TLV700xx-Q1 DDC (5 PINS)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	307.6	262.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	79.1	68.2	
θ_{JB}	Junction-to-board thermal resistance	93.7	81.6	
ψ_{JT}	Junction-to-top characterization parameter	1.3	1.1	
ψ_{JB}	Junction-to-board characterization parameter	92.8	80.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

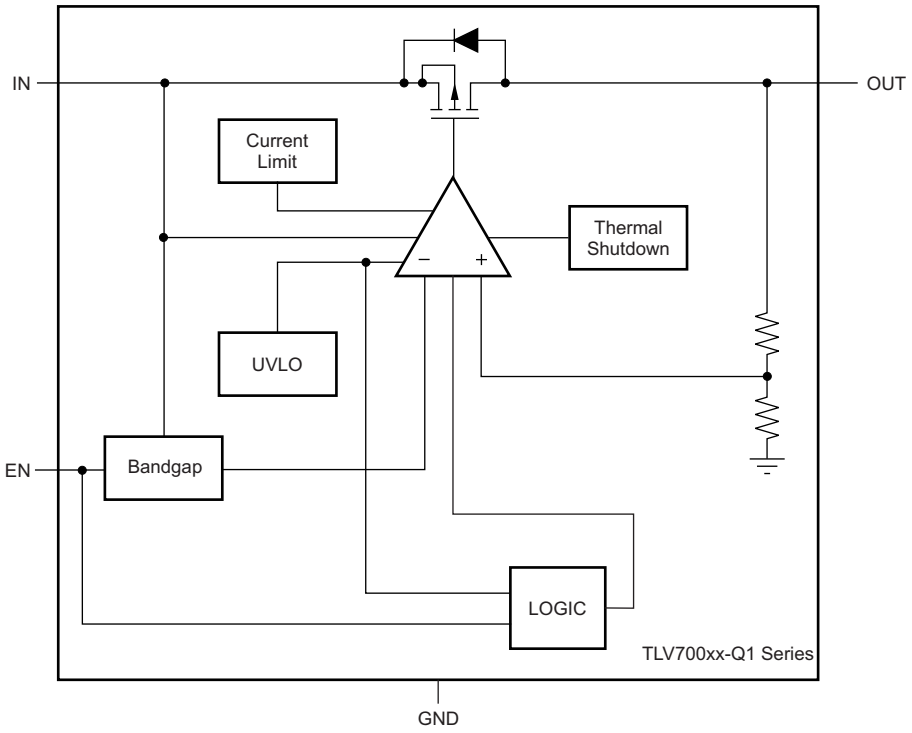
ELECTRICAL CHARACTERISTICS

V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF, and T_A = –40°C to 125°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS		TLV700xx-Q1 MIN	TLV700xx-Q1 TYP	TLV700xx-Q1 MAX	UNIT
V_{IN}	Input voltage range			2		5.5	V
V_{OUT}	DC output accuracy	–40°C ≤ T_A ≤ 125°C	V_{OUT} ≥ 1 V	–2		2	%
			V_{OUT} < 1 V	–20		20	mV
ΔV_O / ΔV_{IN}	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V I_{OUT} = 10 mA			1	5	mV
ΔV_O / ΔI_{OUT}	Load regulation	0 mA ≤ I_{OUT} ≤ 200 mA, TLV70025-Q1 TLV70030-Q1,TLV70033-Q1				15	mV
		0 mA ≤ I_{OUT} ≤ 200 mA, TLV70012A-Q1				20	
V_{DO}	Dropout voltage(1)	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 200 mA			175	250	mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$		220	350	550	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA			31	55	µA
		I_{OUT} = 200 mA, V_{IN} = V_{OUT} + 0.5 V			270		µA
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V			1	2.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V I_{OUT} = 10 mA, f = 1 kHz			68		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			48		μV_{RMS}
t_{STR}	Startup time(2)	C_{OUT} = 1 µF, I_{OUT} = 200 mA			100		µs
$V_{EN(HI)}$	Enable pin high (enabled)			0.9		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)			0		0.4	V
I_{EN}	Enable pin current	V_{EN} = 5.5 V , I_{OUT} = 10 µA			0.04	0.5	µA
UVLO	Undervoltage lockout	V_{IN} rising			1.9		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			160		°C
		Reset, temperature decreasing			140		°C
T_A	Operating ambient temperature			–40		125	°C

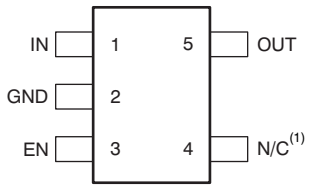
(1) V_{DO} is measured for devices with $V_{OUT(NOM)}$ ≥ 2.35 V.
(2) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

FUNCTIONAL BLOCK DIAGRAM

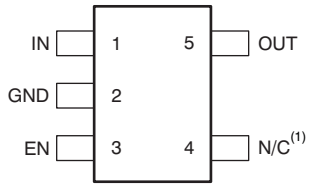


PIN CONFIGURATIONS

TLV700xx-Q1 DDC SOT23-5 PACKAGE (TOP VIEW)



TLV700xx-Q1 DCK SC70-5 PACKAGE (TOP VIEW)



PIN DESCRIPTIONS

NAME	NO.	DESCRIPTION
IN	1	Input pin. A small 1-µF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
GND	2	Ground pin
EN	3	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 µA, nominal.
NC	4	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	5	Regulated output voltage pin. A small 1-µF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

TYPICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

TLV70018
LINE REGULATION

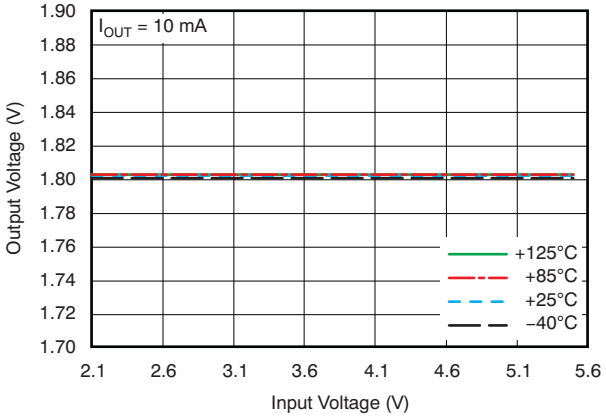


Figure 1.

TLV70018
LINE REGULATION

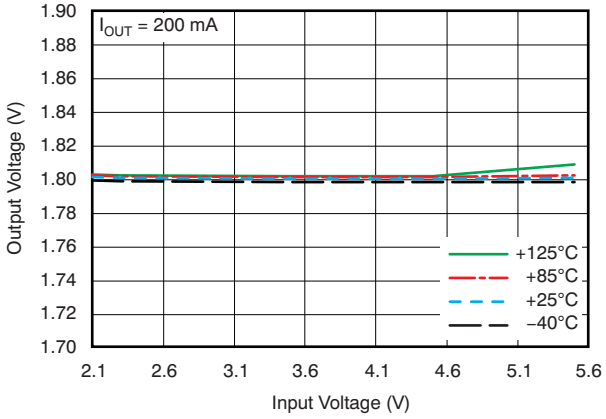


Figure 2.

TLV70018
LOAD REGULATION

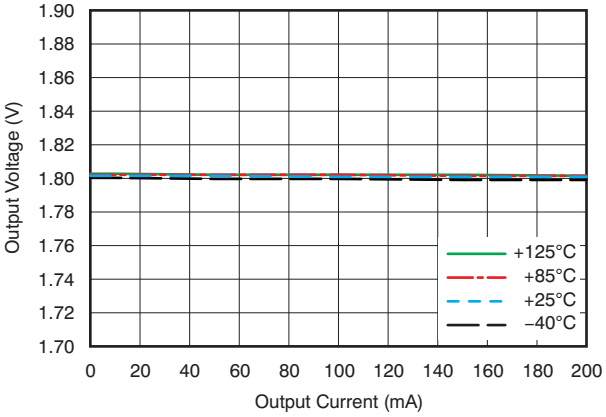


Figure 3.

TLV70048
DROPOUT VOLTAGE vs INPUT VOLTAGE

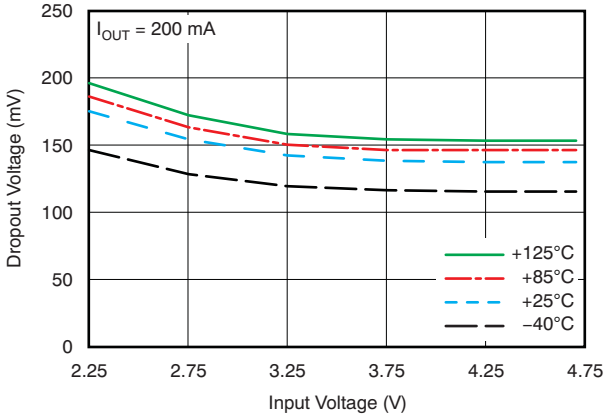


Figure 4.

TLV70048
DROPOUT VOLTAGE vs OUTPUT CURRENT

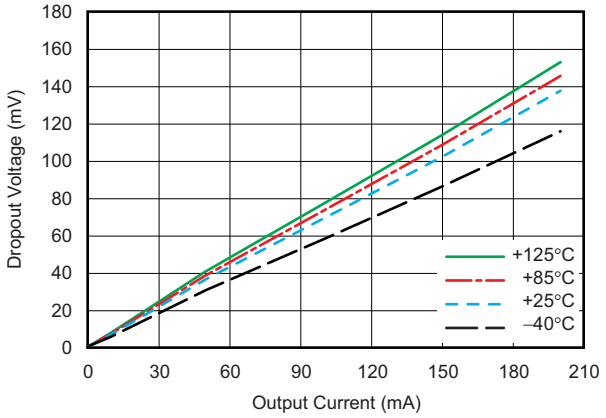


Figure 5.

TLV70018
OUTPUT VOLTAGE vs TEMPERATURE

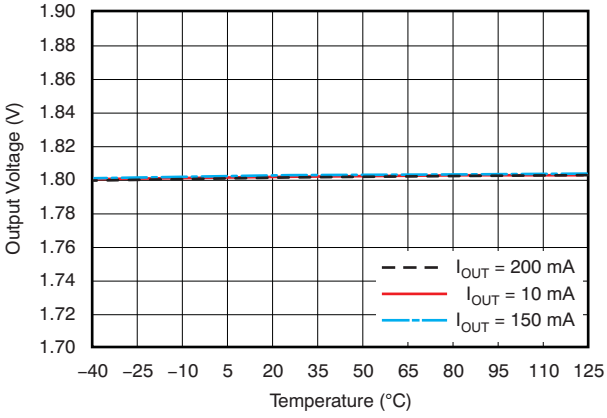


Figure 6.

TYPICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

TLV70018
GROUND PIN CURRENT vs INPUT VOLTAGE

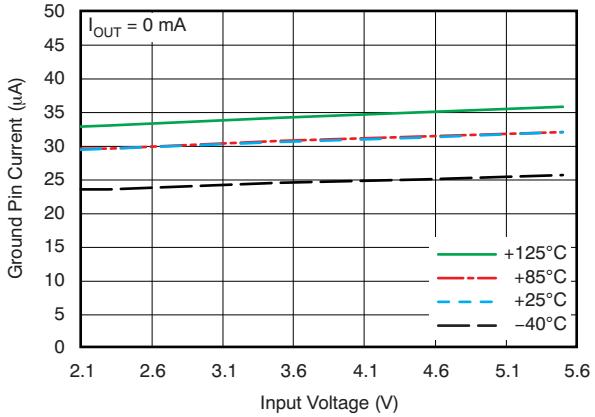


Figure 7.

TLV70018
GROUND PIN CURRENT vs LOAD

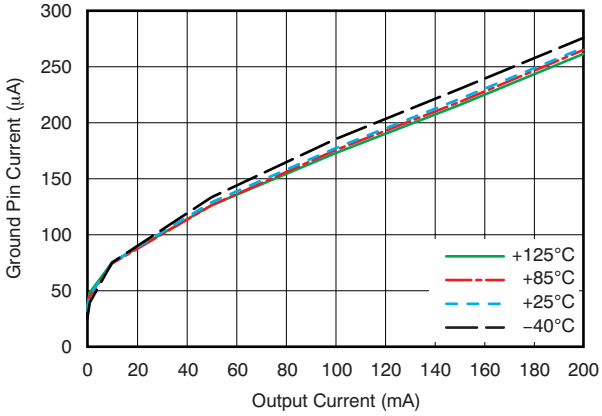


Figure 8.

TLV70018
GROUND PIN CURRENT vs TEMPERATURE

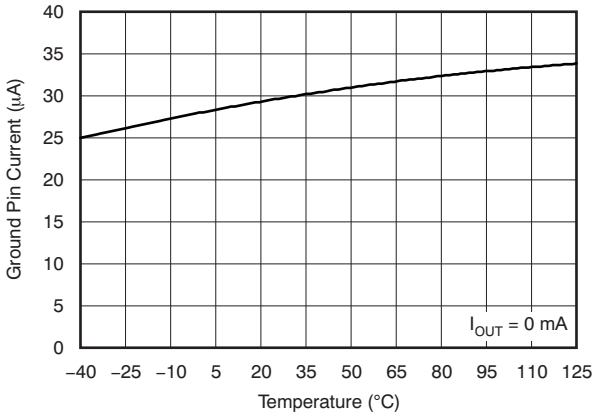


Figure 9.

TLV70018
SHUTDOWN CURRENT vs INPUT VOLTAGE

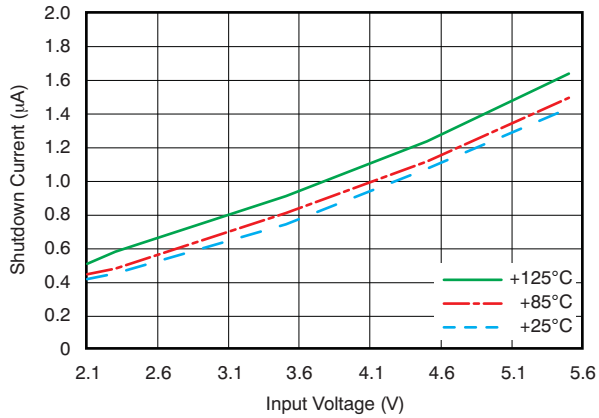


Figure 10.

TLV70018
CURRENT LIMIT vs INPUT VOLTAGE

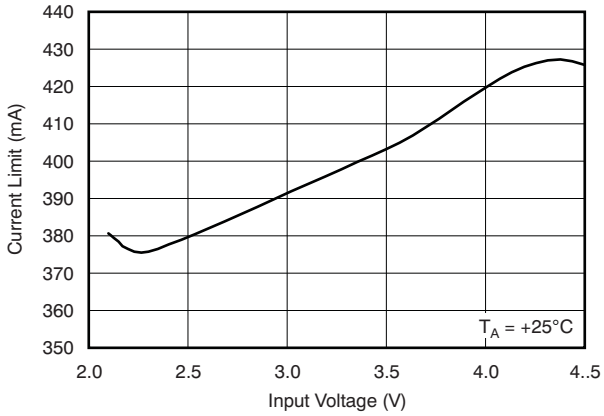


Figure 11.

TLV70018
POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

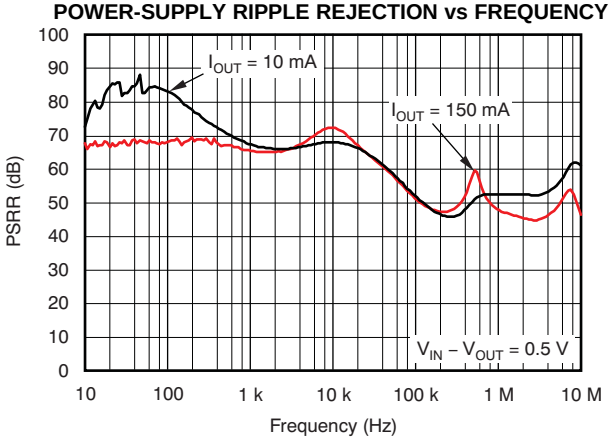


Figure 12.

TYPICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

TLV70018
POWER-SUPPLY RIPPLE REJECTION vs INPUT VOLTAGE

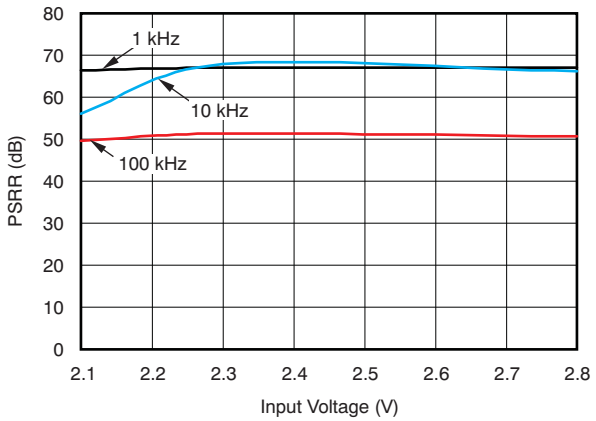


Figure 13.

TLV70018
OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT VOLTAGE

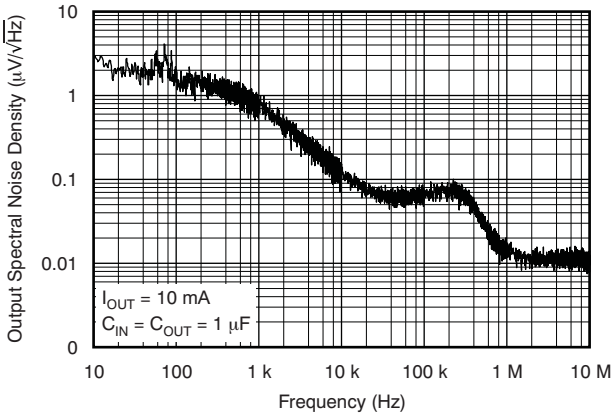


Figure 14.

TLV70018
LOAD TRANSIENT RESPONSE

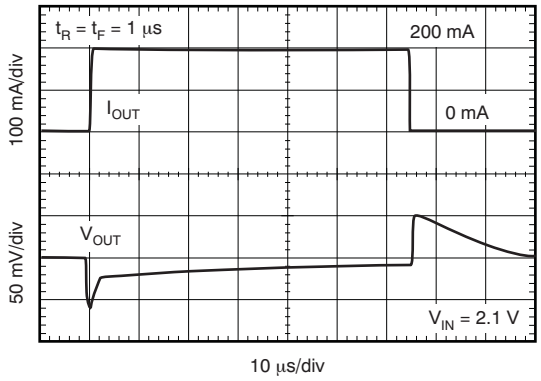


Figure 15.

TLV70018
LOAD TRANSIENT RESPONSE

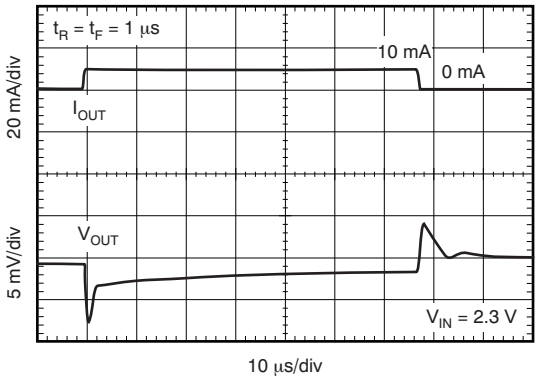


Figure 16.

TLV70018
LOAD TRANSIENT RESPONSE

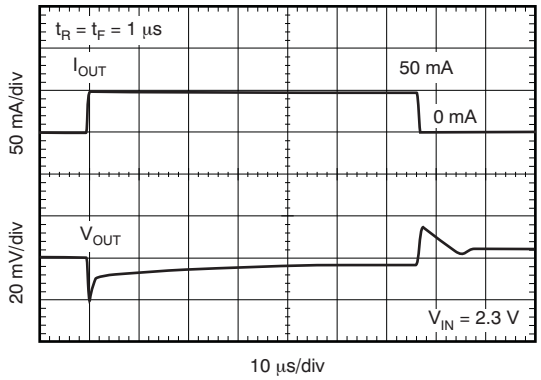


Figure 17.

TLV70018
LINE TRANSIENT RESPONSE

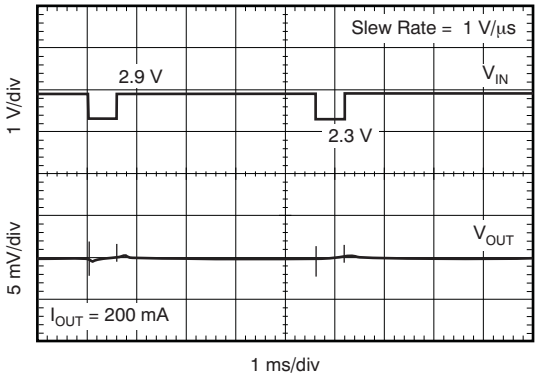


Figure 18.

TYPICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1 µF (unless otherwise noted). Typical values are at T_J = 25°C.

TLV70018
LINE TRANSIENT RESPONSE

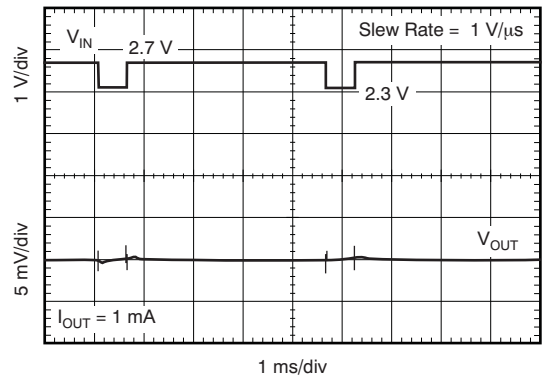


Figure 19.

TLV70018
LINE TRANSIENT RESPONSE

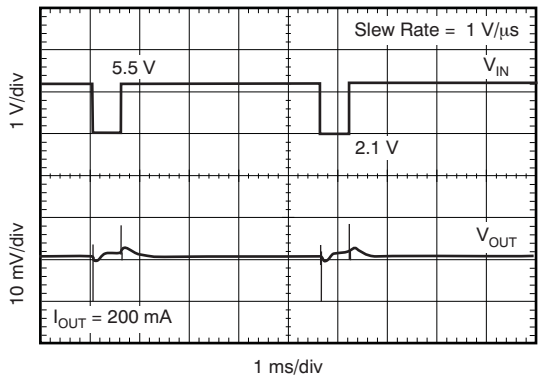


Figure 20.

TLV70018
V_{IN} RAMP UP, RAMP DOWN RESPONSE

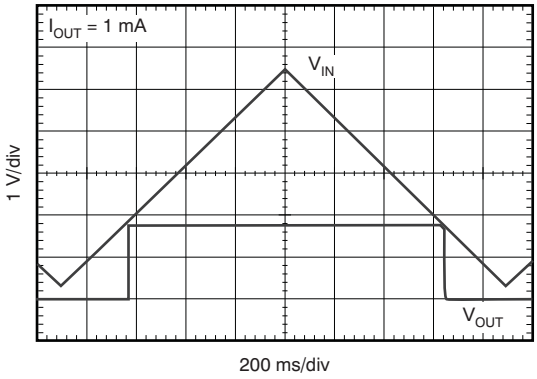


Figure 21.

APPLICATION INFORMATION

The TLV700xx-Q1 belongs to a new family of next-generation value LDO regulators. It consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this device ideal for RF portable applications. This family of regulators offers subband-gap output voltages down to 0.7 V, current limit, and thermal protection, and is specified from –40°C to 125°C.

Input and Output Capacitor Requirements

1.0-µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV700xx-Q1 is designed to be stable with an *effective capacitance* of 0.1 µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller-footprint capacitors that have higher derating in size- and space-constrained applications.

Note that using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF, low-ESR capacitor across the IN pin and GND in of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High-ESR capacitors may degrade PSRR performance.

Internal Current Limit

The TLV700xx-Q1 internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates (V_{IN} – V_{OUT}) × I_{LIMIT} until thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal-shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the Thermal Information section for more details.

The PMOS pass element in the TLV700xx-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Shutdown

The enable pin (EN) is active-high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin.

Dropout Voltage

The TLV700xx-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $r_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 13 in the Typical Characteristics section.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over-/undershoot magnitude but increases the duration of the transient response.

Undervoltage Lockout (UVLO)

The TLV700xx-Q1 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly.

Thermal Information

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV700xx-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV700xx-Q1 into thermal shutdown degrades device reliability.

REVISION HISTORY

Changes from Revision E (January 2013) to Revision F **Page**

- Changed CDM classification level from C3B to C4B in FEATURES list 1
- Changed ambient temperature range in *ABSOLUTE MAXIMUM RATINGS* table 2
- Added Electrostatic discharge ratings to *Absolute Maximum Ratings* table 2
- Changed Ground pin current (shutdown) max value from 2 to 2.5 in *Electrical Characteristics* table 3
- Added TLV70028-Q1 and TLV70032-Q1 to document 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV70012QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDX	Samples
TLV70025QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QVC	Samples
TLV70028QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJU	Samples
TLV70030QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDW	Samples
TLV70032QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKA	Samples
TLV70033QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

OTHER QUALIFIED VERSIONS OF TLV70025-Q1, TLV70028-Q1, TLV70030-Q1, TLV70032-Q1, TLV70033-Q1 :

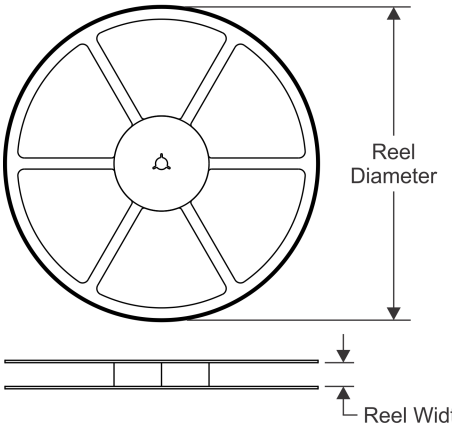
- Catalog: TLV70025, TLV70028, TLV70030, TLV70032, TLV70033

NOTE: Qualified Version Definitions:

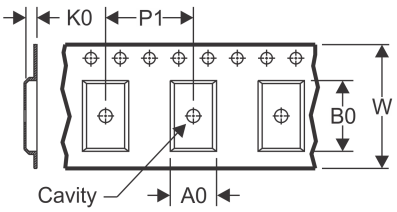
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

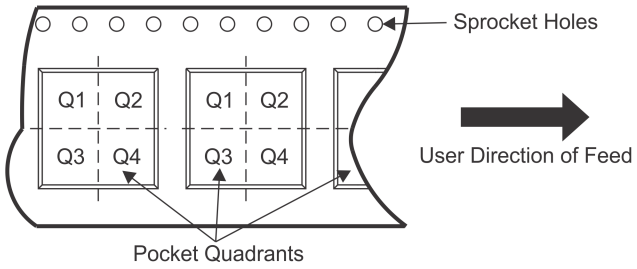


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

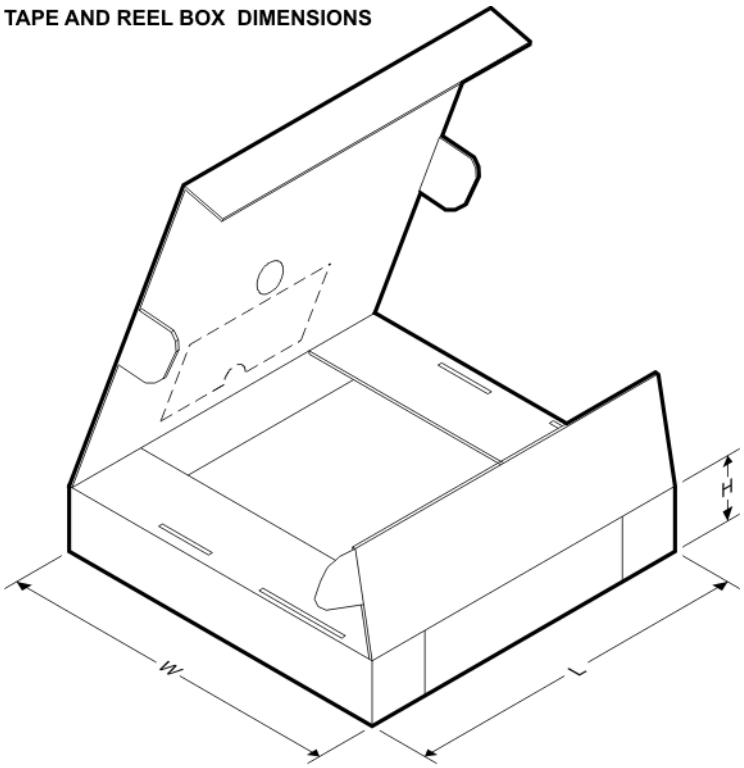
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70012QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV70025QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70028QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70032QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70033QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

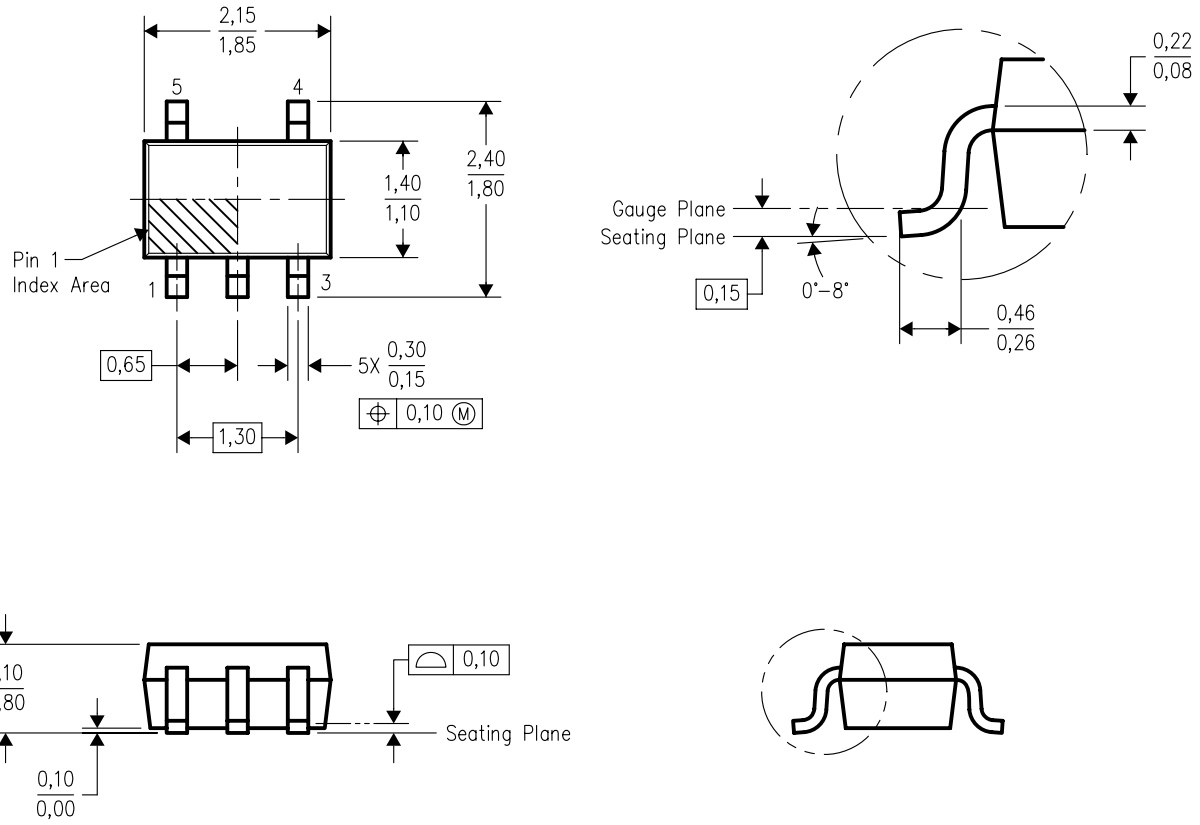
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70012QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
TLV70025QDDCRQ1	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70028QDDCRQ1	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70032QDDCRQ1	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70033QDDCRQ1	SOT	DDC	5	3000	195.0	200.0	45.0

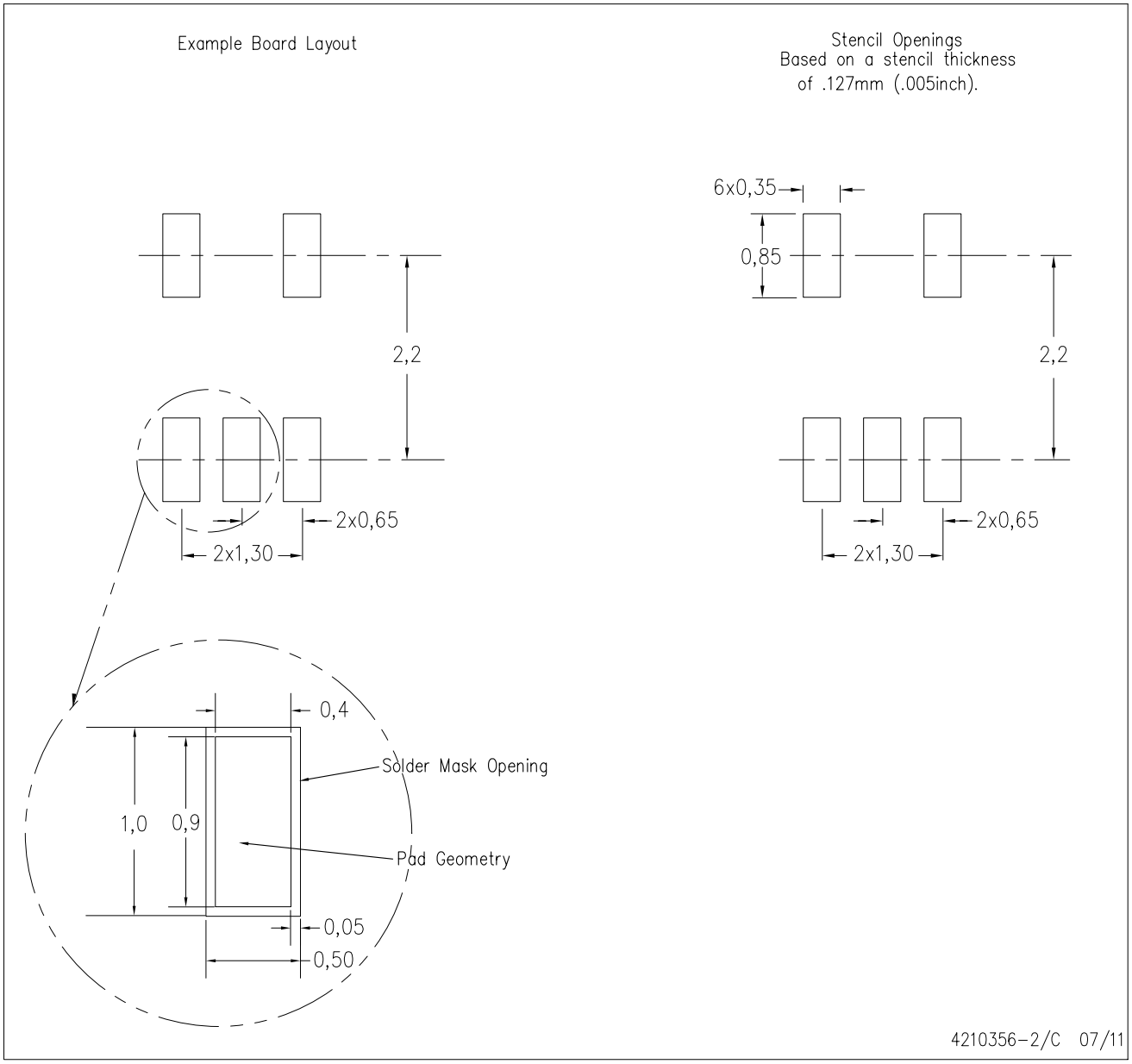
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

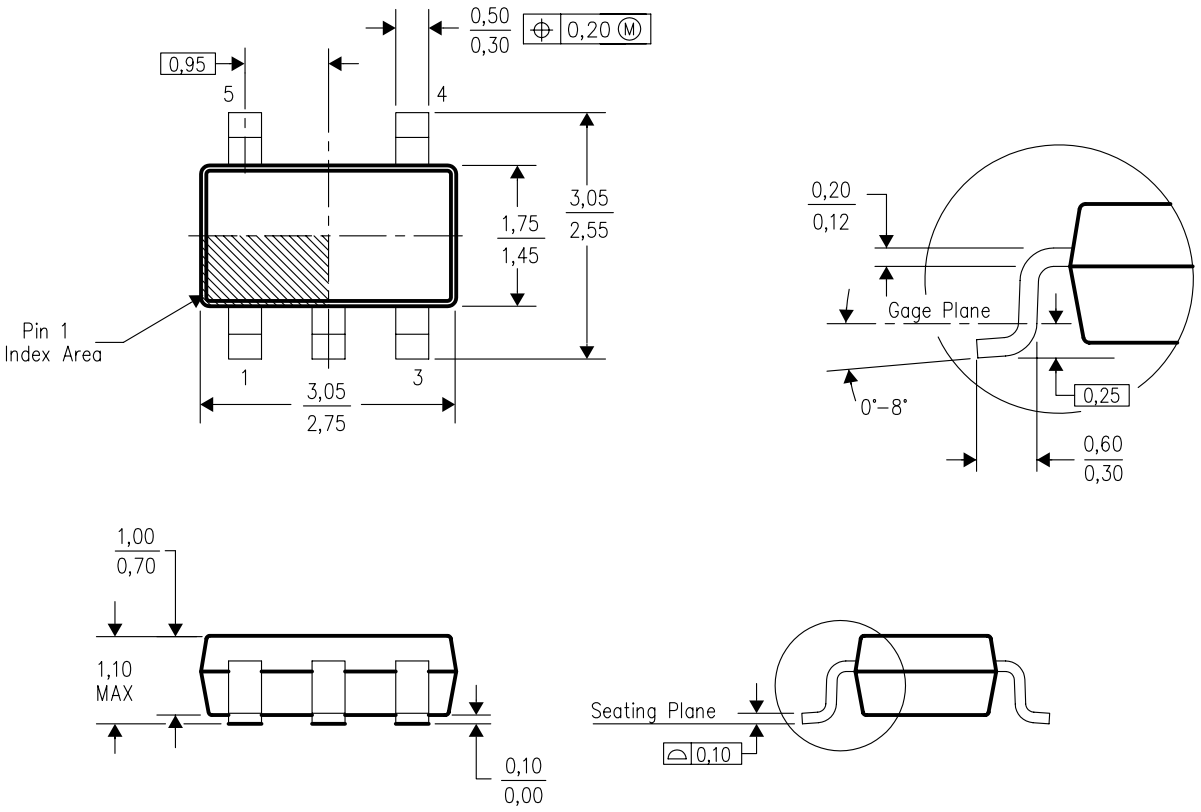
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

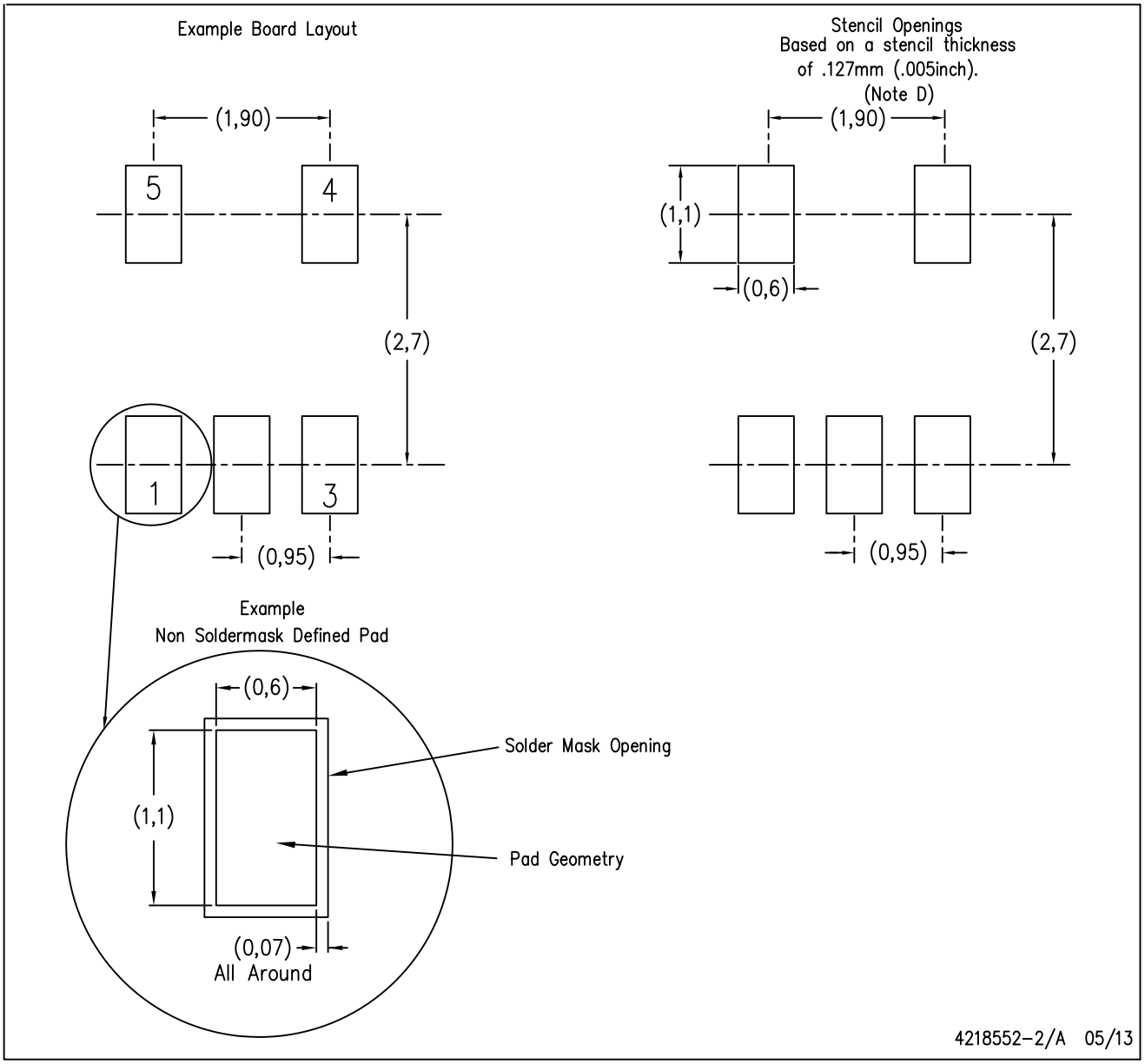
DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



4204403–2/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DDC (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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