AS3935

Franklin Lightning Sensor IC

General Description

The AS3935 is a programmable fully integrated Lightning Sensor IC that detects the presence and approach of potentially hazardous lightning activity in the vicinity and provides an estimation on the distance to the head of the storm. The embedded lightning algorithm checks the incoming signal pattern to reject the potential man-made disturbers.

The AS3935 can also provide information on the noise level and inform the external unit (e.g. microcontroller) in case of high noise conditions, with the noise floor generator and noise floor evaluation blocks.

The AS3935 can be programmed via a 4-wire standard SPI or an I^2C. Also, in case the latter is chosen, it is possible to choose among three different addresses. Two clocks are internally generated by two different RC-Oscillators: TRCO and SRCO. An automatic calibration procedure can increase the precision of those oscillators. The AS3935 can be either supplied by an internal voltage regulator or directly by VDD.

For further understanding in regards to the contents of the datasheet, please refer to the Reference Guide located at the end of the document.

Key Benefits & Features

The benefits and features of AS3935, Franklin Lightning Sensor IC are listed below:

Figure 1:
Added Value of using AS3935

Benefits	Features
Advanced warning ahead of human senses	Lightning sensor warns of lightning storm activity within a radius of 40km
Early awareness of approaching storms	Distance estimation to the head of the storm down to 1km in 14 steps
Detection of both types of lightning phenomena	Detects both cloud-to-ground and intra-cloud (cloud-to-cloud) flashes
Reduces false detections	Embedded man-made disturber rejection algorithm
Flexibility for various applications	Programmable detection levels enable threshold setting for optimal controls
Flexibility w industry standard interfaces	SPI and I^2C interface is used for control and register reading

Benefits	Features
Ensures optimal receive performance	Antenna Tuning to compensate variations of the external components
Flexible supply range	Supply voltage range 2.4V to 5.5V
Configurability of power modes	Power-down, listening, and active mode
Very small package size	Package: 16LD MLPQ (4x4mm)

Applications

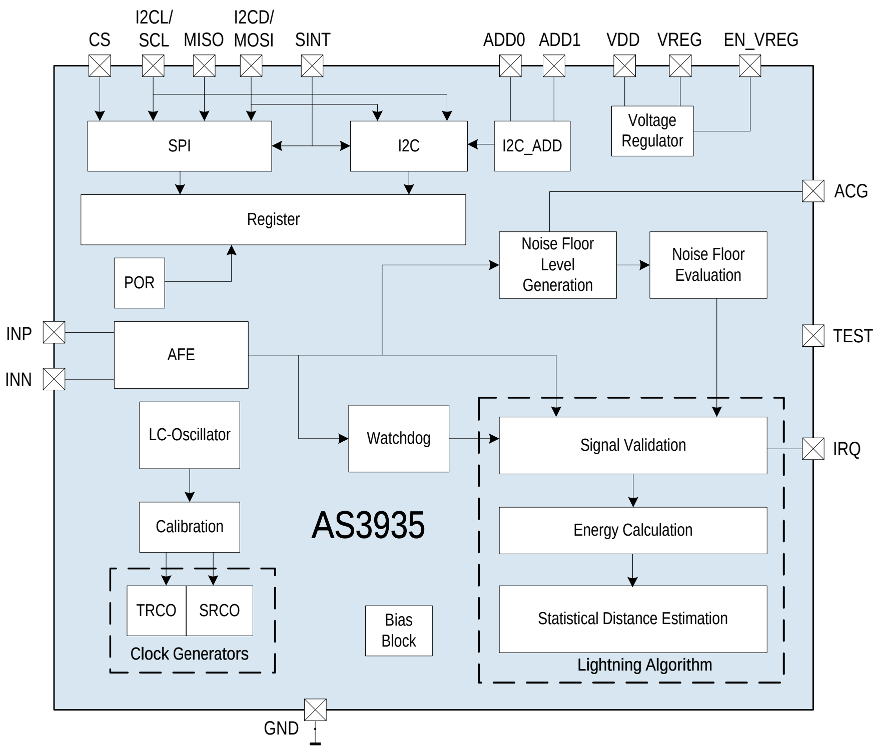
AS3935 is ideal for:

- Weather Stations
- Clocks
- Sports Equipment
- Portables
- Pool Safety
- Uninterruptible Power Supply (UPS)
- Global Positioning System (GPS)
- Cellular phones
- Watches
- Golf Equipment

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
AS3935 Block Diagram



Pin Assignments

The AS3935 Pin assignments are shown below.

Figure 3:
Pin Diagram of AS3935 (Top View)

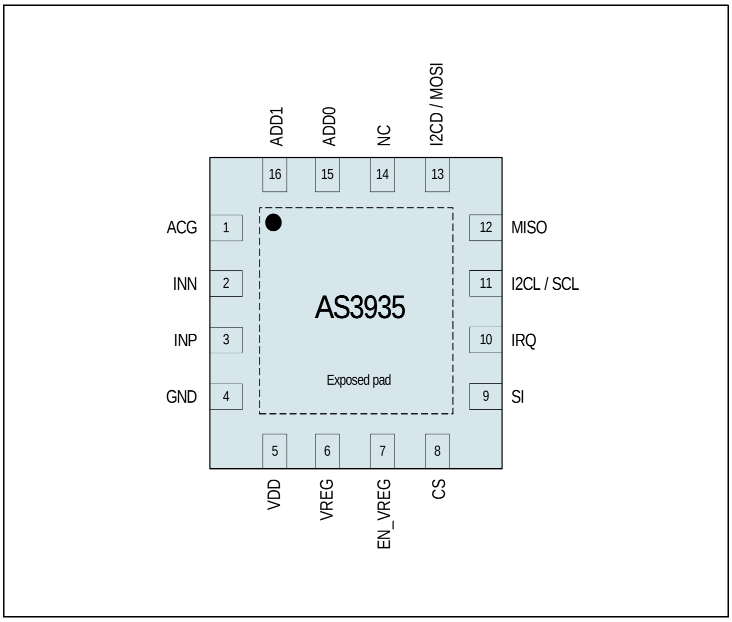


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	ACG	Analog I/O	AC-Ground
2	INN		Antenna ground
3	INP		Antenna positive input
4	GND	Supply pad	Ground
5	VDD		Positive supply voltage
6	VREG		Positive supply voltage / Regulated voltage
7	EN_VREG	Digital input	Voltage Regulator Enable
8	CS		Chip Select (active low)
9	SI		Select Interface (GND → SPI or VDD → I²C)
10	IRQ	Digital output	Interrupt
11	I2CL/SCL	Digital input	I²C clock bus or SPI clock bus (according to SI setting)
12	MISO	Digital output	SPI data output bus
13	I2CD/MOSI	Digital I/O with pull-up / Digital input	I²C data bus or SPI data input bus (according to SI setting)

Pin Number	Pin Name	Pin Type	Description
14	NC		Not connected
15	ADD0	Digital input	I^2C address selection LSB
16	ADD1		I^2C address selection MSB
Exposed pad		Supply pad	Connect to Ground via the GND plan and pin 4

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" on page 7 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD	DC supply voltage	-0.5	7	V	
VIN	Input pin voltage	-0.5	5	V	
I_{scr}	Input current (latch up immunity)	-100	100	mA	Norm: Jedec 78
Electrostatic Discharge					
ESD	Electrostatic discharge	±2		kV	Norm: MIL 883 E method 3015 (Human Body Model)
Continuous Power Dissipation					
P_t	Total power dissipation (all supplies and outputs)		0.1	mW	
Temperature Ranges and Storage Conditions					
T_{strg}	Storage temperature	-65	150	ºC	
T_{body}	Package body temperature		260	ºC	Norm: IPC/JEDEC J-STD-020 The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices".
	Humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Operating Conditions

All defined tolerances for external components in this specification need to be assured over the whole operation condition range and also over lifetime.

Figure 6:
Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Positive supply voltage	In case the voltage regulator is ON	2.4		5.5	V
		In case the voltage regulator is OFF	2.4		3.6	V
T_{AMB}	Ambient temperature		-40		85	ºC

DC/AC Characteristics for Digital Inputs and Outputs

Figure 7:
CMOS Input

Symbol	Parameter	Min	Typ	Max	Units
V_{IH}	High level input voltage	0.6*VDD	0.7*VDD	0.9*VDD	V
V_{IL}	Low level input voltage	0.125*VDD	0.2*VDD	0.3*VDD	V

Note: On ALL outputs, use the cells with the smallest drive capability which will do the job, in order to prevent current/spikes problems.

Figure 8:
CMOS Output

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage	With a load current of 1mA	VDD-0.4			V
V_{OL}	Low level output voltage				VSS+0.4	V
CL	Capacitive load	For a clock frequency of 1MHz			400	pF

Figure 9:
Tristate CMOS Output

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage	With a load current of 1mA	VDD-0.4			V
V_{OL}	Low level output voltage				VSS+0.4	V
IOZ	Tristate leakage current	To V_{DD} and V_{SS}			400	nA

Detailed System and Block Specification

Figure 10:
Electrical System Specifications

Symbol	Parameter	Min	Typ	Max	Units	Note
Input Characteristic						
R_{IN}	Input AC impedance		200		kΩ	
Current Consumption						
$I_{PWDROFF}$	Power-down current when VREG is OFF		1	2	µA	
I_{PWDRON}	Power-down current when VREG is ON		8	15	µA	
$I_{LSMROFF}$	Current consumption in listening mode when VREG is OFF		60	80	µA	
I_{LSMRON}	Current consumption in listening mode when VREG is ON		70		µA	
I_{SVM}	Current Consumption in signal verification mode		350		µA	
Timing						
$T_{lightning}$	Duration in signal verification mode once lightning is detected		1		s	
$T_{disturber}$	Duration in signal verification mode once disturber is detected		1.5		s	

Symbol	Parameter	Min	Typ	Max	Units	Note
Oscillators						
LCO_{SUT}	LCO Start-up Time			2	ms	Time needed by the LCO to start-up
T_{SRCO}	SRCO frequency after calibration	1.065	1.125	1.19	MHz	Assuming FLCO = 500 kHz
T_{TRCO}	TRCO frequency after calibration	30.5	32.26	34.0	kHz	
TRCOCAL	Calibration time for the RC oscillators			2	ms	The calibration of the RC oscillators starts after the LCO settles
Voltage Regulator						
VR_{OUT}	Voltage regulator output voltage	2.7	3.0	3.3	V	

Typical Operating Characteristics

Figure 11:
Power-down current if Voltage Regulator is OFF over Supply Voltage (VREG)

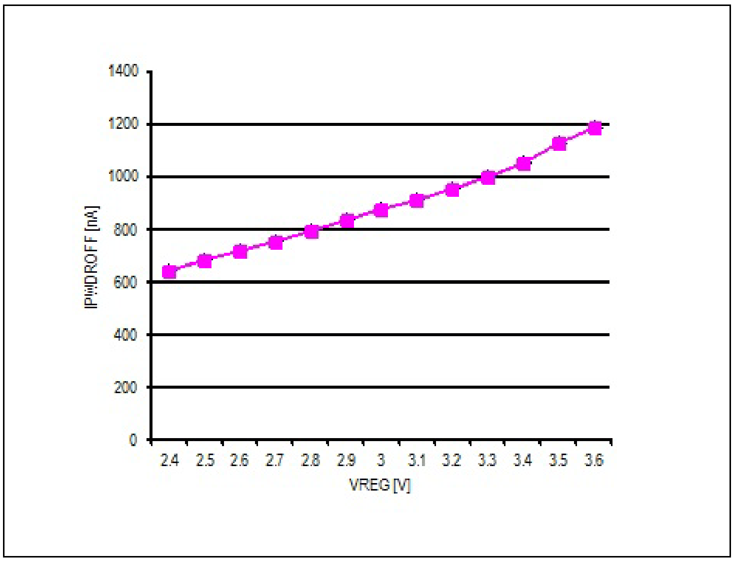


Figure 12:
Power-down Current if Voltage Regulator is OFF @3V over Temperature

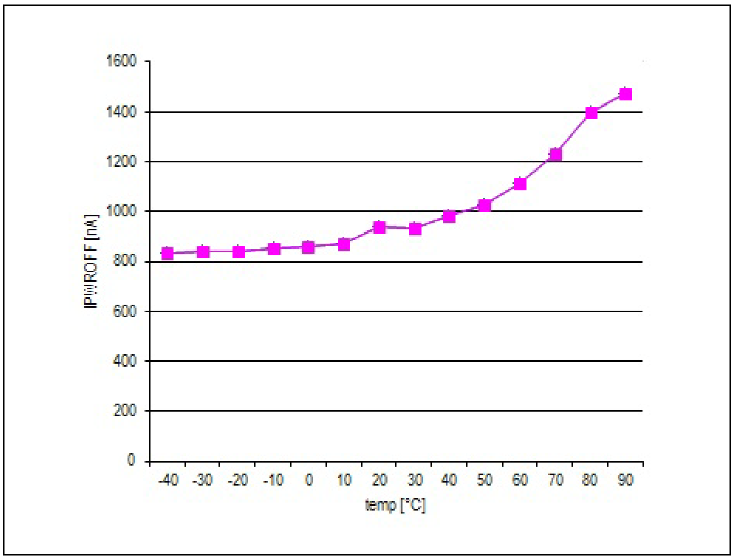


Figure 13:
Current Consumption in Listening Mode if Voltage Regulator is OFF over Supply Voltage (VREG)

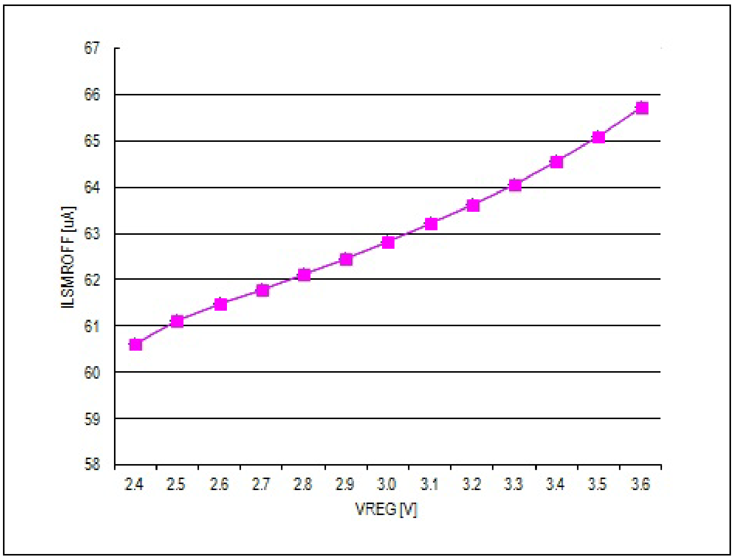


Figure 14:
Current Consumption in Listening Mode if Voltage Regulator is OFF over Temperature (@ VREG=3V)

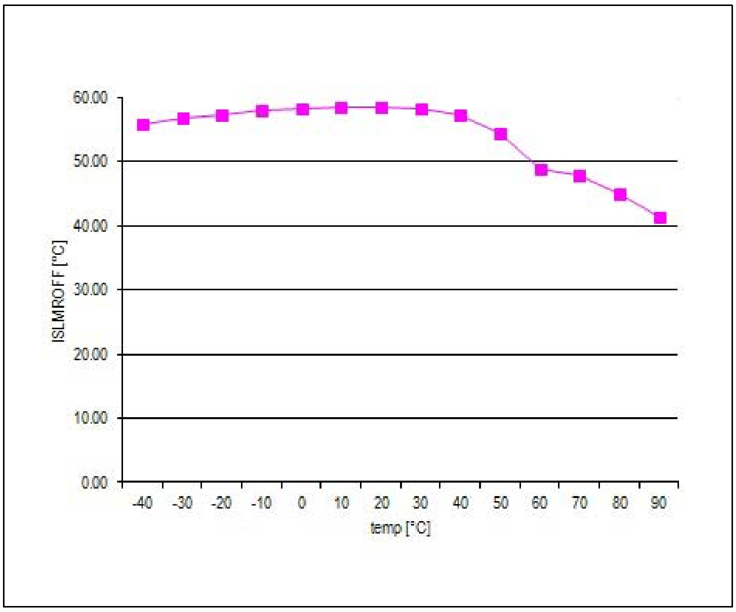


Figure 15:
Output Regulated Voltage (VREG) @VDD=5V over Temperature

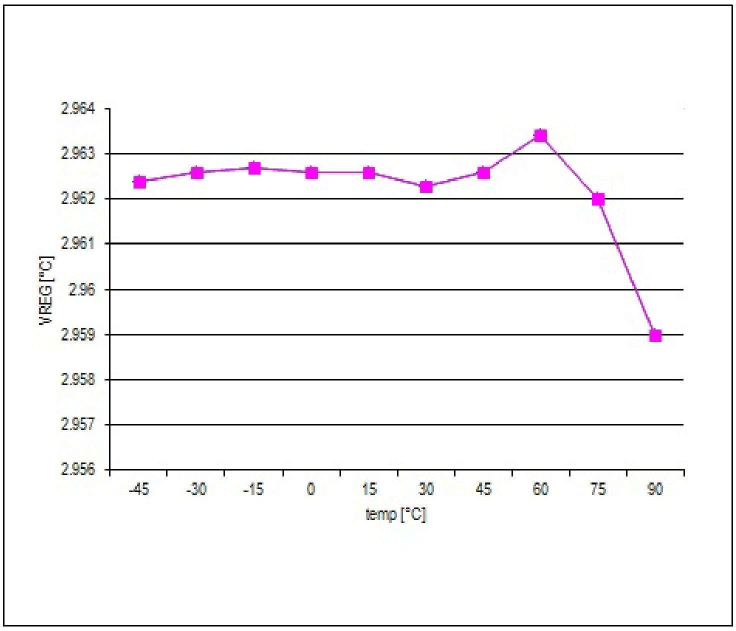
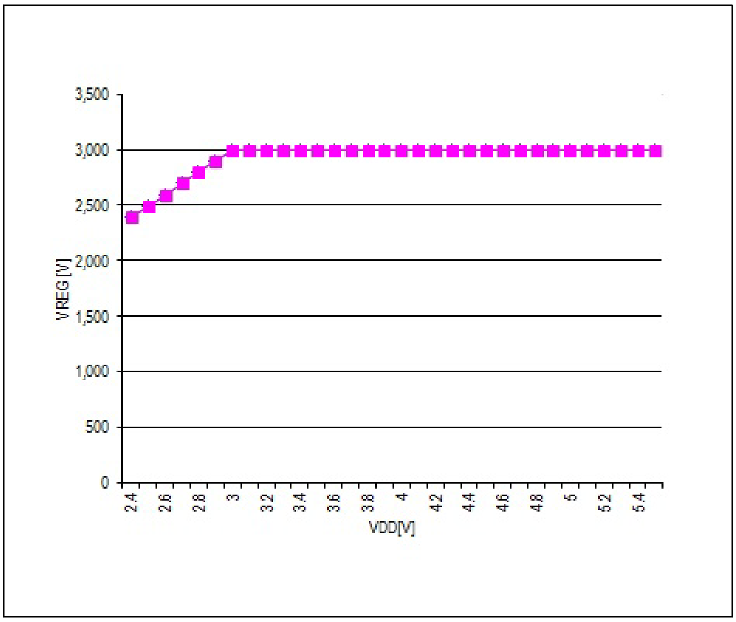


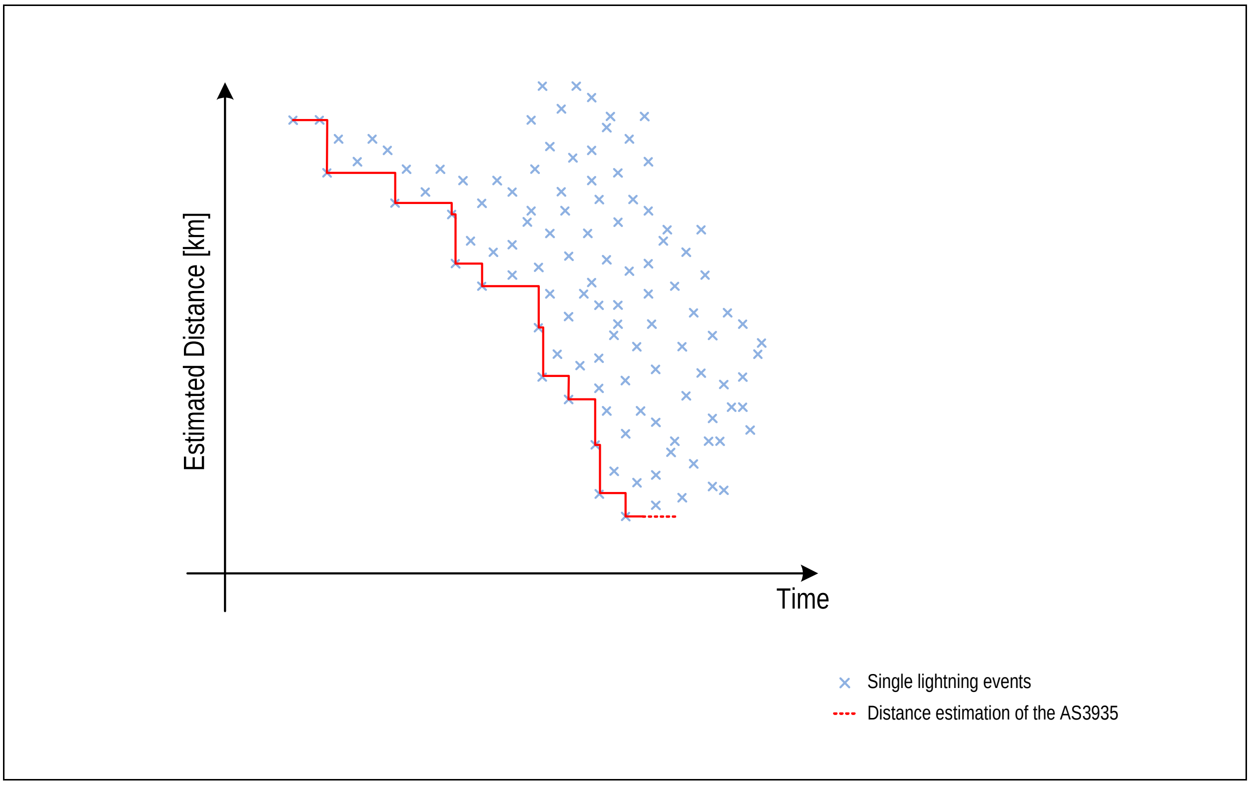
Figure 16:
Output Regulated Voltage (VREG) @ Room Temperature over Supply Voltage



Detailed Description

The AS3935 can detect the presence of an approaching storm with lightning activities and provide an estimation of the distance to the leading edge of the storm, where the leading edge of the storm is defined as the minimum distance from the sensor to the closest edge of the storm. The embedded hardwired distance estimation algorithm of the AS3935 issues an interrupt on the IRQ pin (see Interrupt Management on page 34) every time a lightning is detected. The estimated distance which is displayed in the distance estimation register does not represent the distance to the single lightning but the estimated distance to the leading edge of the storm. A graphical representation is shown in the Figure 17.

Figure 17:
Storm



As shown in Figure 18, Figure 19, Figure 20, and Figure 21, the system integration consists mainly of the AS3935 and an external control unit (e.g. MCU) for the IC initialization and interrupt management (IRQ).

The choice of interface type (SPI vs. I²C) is accomplished using pin 9, SI (Select Interface). When the SI is connected to GND, the SPI is selected. When the SI is connected to VDD, the I²C is selected. Pins ADD0 and ADD1 are used to select among 3 different I²C address.

The internal voltage regulator can be enabled by connecting EN_VREG to VDD. If the internal regulator is not used, capacitor C3 is not needed and VREG must be connected to VDD. In this case, the AS3935 can be directly supplied by VREG and VDD (EN_VREG to GND).

AS3935 needs the following external components:

- Power supply capacitor – CBAT – 1µF.
- Load capacitor on the ACG and VREG pins; the latter is needed only in case the voltage regulator is enabled.
- RLC resonator as antenna.
- One resistor on the I2CL pin to VDD, if I²C is active (R2 > 10kΩ).

Figure 18:
AS3935 Application Diagram (Voltage Regulator OFF, SPI Active)

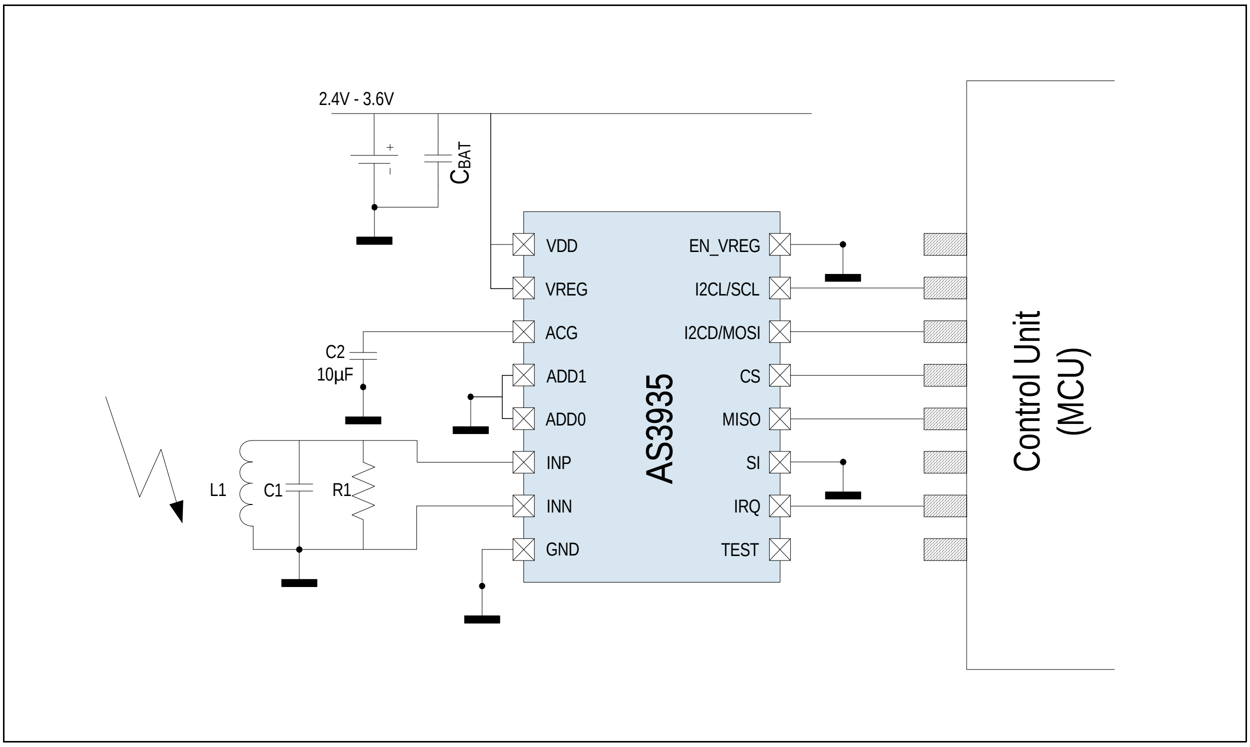


Figure 19:
AS3935 Application Diagram (Voltage Regulator OFF, I²C Active)

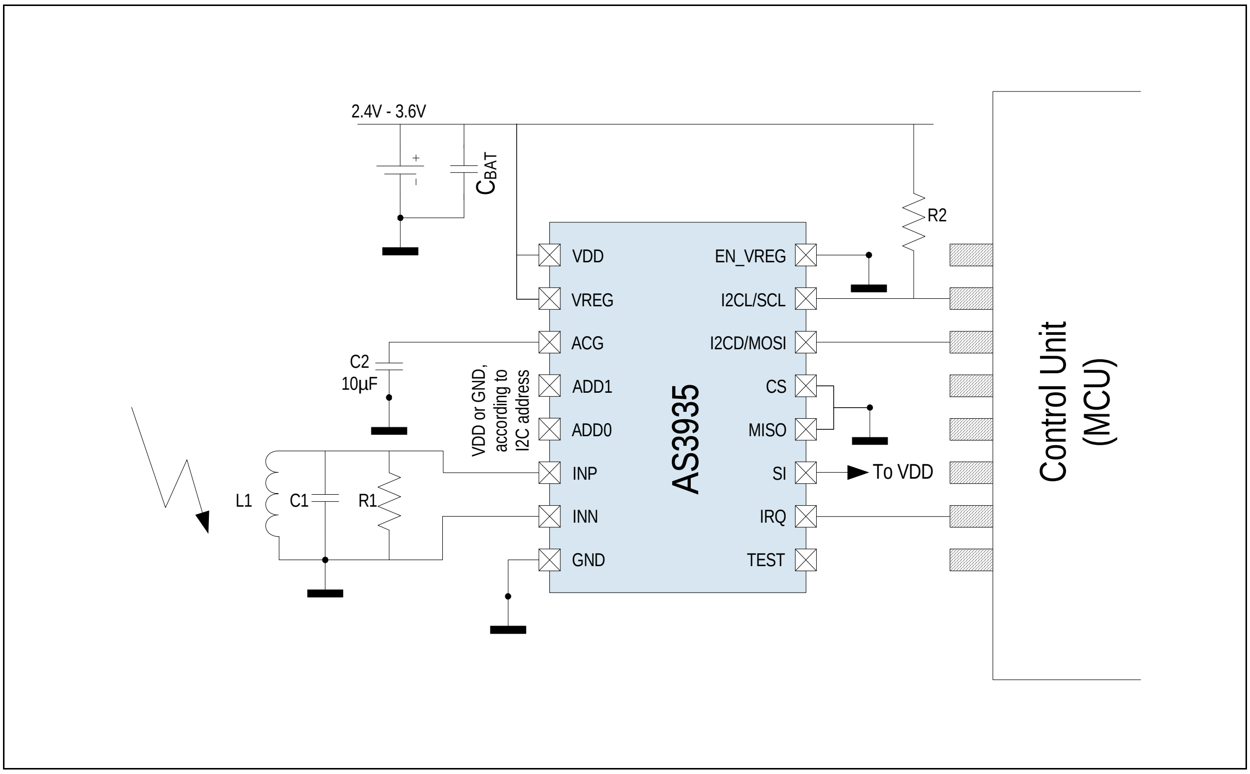


Figure 20:
AS3935 Application Diagram (Voltage Regulator ON, SPI Active)

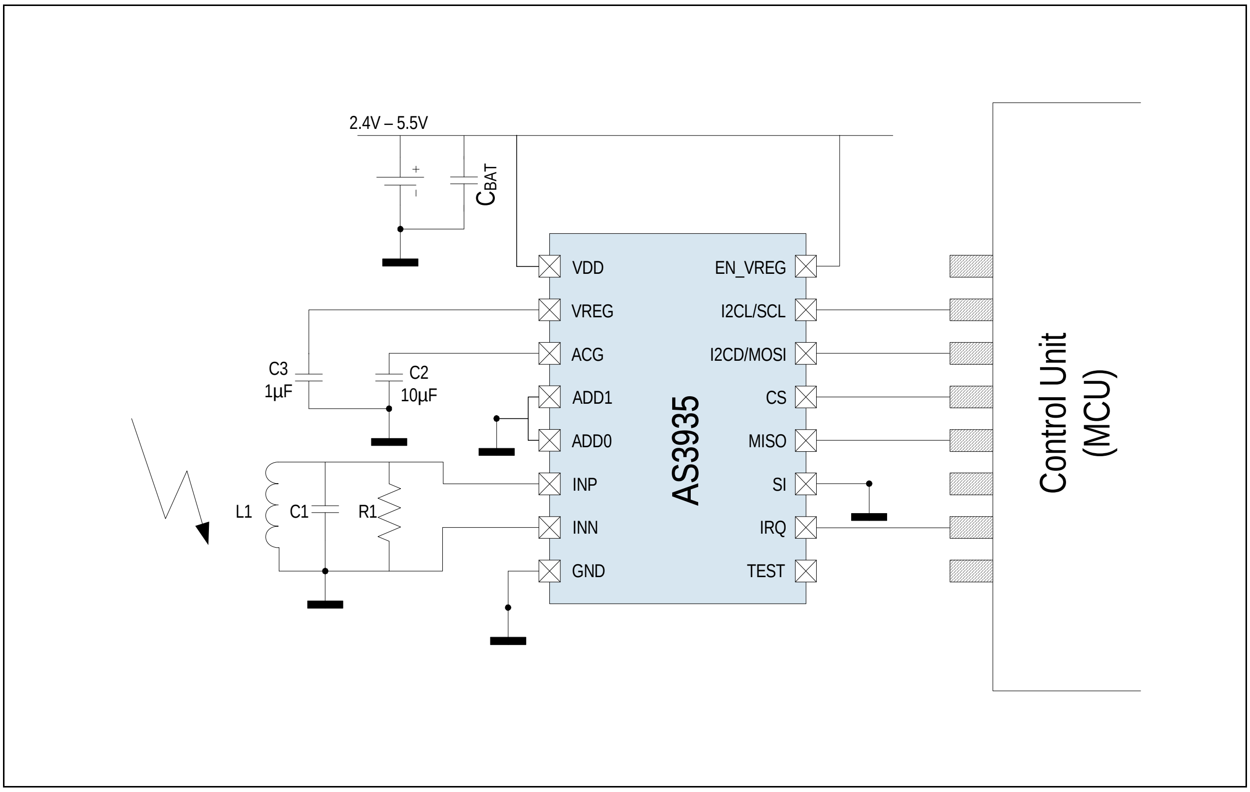
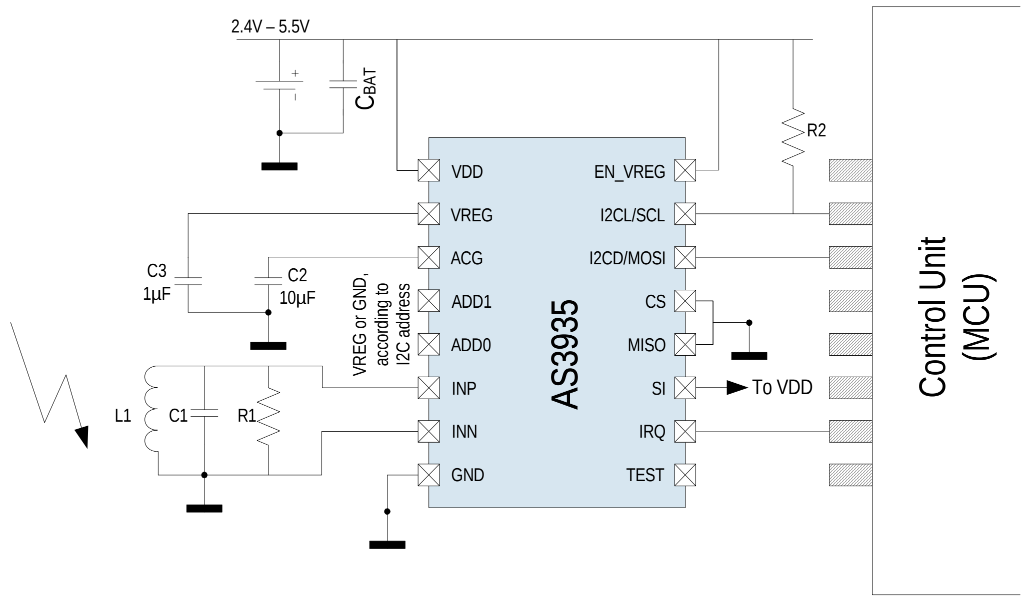


Figure 21:
AS3935 Application Diagram (Voltage Regulator ON, I²C Active)



Circuit

Figure 2 shows a block diagram of the AS3935. The external antenna is directly connected to the Analog Front-end (AFE), which amplifies and demodulates the received signal. The watchdog continuously monitors the output of the AFE and alerts the integrated lightning algorithm block in the event of an incoming signal. The lightning algorithm block validates the signal by checking the signal pattern. It is capable of distinguishing between signals caused by lightning strikes and signals caused by man-made noise sources, so called disturbers. In case the signal is classified as man-made disturber, the event is rejected and the sensor automatically goes back to listening mode. Is the event classified as lightning strike, the statistical distance estimation block performs an estimation of the distance to the head of the storm.

The LC oscillator together with the calibration block can calibrate both the TRCO and the SRCO clock generator to compensate process variations.

Operating Modes

Power-down Mode

In Power-down Mode, the entire AS3935 is switched off to reduce the current consumption to minimum (typ 1µA).

Listening Mode

In listening mode the AFE, the watchdog, the noise floor level generation, the bias block, the TRCO, and the voltage regulator (in case it is enabled) are running. In this mode the system can push down the power consumption to a minimum (typ 60µA). In case the maximum voltage supply does not exceed 3.6V, it is possible to switch off the voltage regulator to save power.

Signal Verification

The signal verification mode is based on the Lightning Algorithm block, which is shown in Figure 2 and described in more detail in section Lightning Algorithm. Every time the watchdog threshold is passed the AS3935 enters the signal verification mode. The watchdog threshold can be set in **REG0x01[3:0]**. If the signal is classified as disturber the chip immediately aborts the signal processing and goes back into the listening mode. Otherwise, the energy calculation is performed and the distance estimate provided.

System and Block Specification

Register Table

Figure 22:
Register Table

<table>
<tr><th>Register #</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0x00</td><td colspan="2">Reserved</td><td colspan="5">AFE_GB</td><td>PWD</td></tr>
<tr><td>0x01</td><td>Reserved</td><td colspan="3">NF_LEV</td><td colspan="4">WDTH</td></tr>
<tr><td>0x02</td><td>Reserved</td><td>CL_STAT</td><td colspan="2">MIN_NUM_LIGH</td><td colspan="4">SREJ</td></tr>
<tr><td>0x03</td><td colspan="2">LCO_FDIV</td><td>MASK_DIST</td><td>Reserved</td><td colspan="4">INT</td></tr>
<tr><td>0x04</td><td colspan="8">S_LIG_L</td></tr>
<tr><td>0x05</td><td colspan="8">S_LIG_M</td></tr>
<tr><td>0x06</td><td colspan="3">Reserved</td><td colspan="5">S_LIG_MM</td></tr>
<tr><td>0x07</td><td colspan="2">Reserved</td><td colspan="6">DISTANCE</td></tr>
<tr><td>0x08</td><td>DISP_LCO</td><td>DISP_SRCO</td><td>DISP_TRCO</td><td>Reserved</td><td colspan="4">TUN_CAP</td></tr>
<tr><td>0x3A</td><td>TRCO_CALIB_DONE</td><td>TRCO_CALIB_NOK</td><td colspan="6">Reserved</td></tr>
<tr><td>0x3B</td><td>SRCO_CALIB_DONE</td><td>SRCO_CALIB_NOK</td><td colspan="6">Reserved</td></tr>
</table>

Register Table Description and Default Value

Figure 23:
Detailed Register Map

Address	Register Name	Bit	Type	Default Value	Description
0x00	Reserved	[7:6]	R/W	0	Reserved
	AFE_GB	[5:1]		10010	AFE Gain Boost
	PWD	[0]		0	Power-down
0x01	NF_LEV	[6:4]	R/W	010	Noise Floor Level
	WDTH	[3:0]		0010	Watchdog threshold
0x02	Reserved	[7]	R/W	1	Reserved
	CL_STAT	[6]		1	Clear statistics
	MIN_NUM_LIGH	[5:4]		00	Minimum number of lightning
	SREJ	[3:0]		0010	Spike rejection
0x03	LCO_FDIV	[7:6]	R/W	00	Frequency division ration for antenna tuning
	MASK_DIST	[5]		0	Mask Disturber
	Reserved	[4]		0	Reserved
	INT	[3:0]	R	0000	Interrupt (see Figure 43)
0x04	S_LIG_L	[7:0]	R	00000000	Energy of the Single Lightning LSBYTE
0x05	S_LIG_M	[7:0]	R	00000000	Energy of the Single Lightning MSBYTE
0x06	Reserved	[7:5]			Reserved
	S_LIG_MM	[4:0]	R	00000	Energy of the Single Lightning MMSBYTE
0x07	Reserved	[7:6]			Reserved
	DISTANCE	[5:0]	R	000000	Distance estimation
0x08	DISP_LCO	[7]	R/W	0	Display LCO on IRQ pin
	DISP_SRCO	[6]		0	Display SRCO on IRQ pin
	DISP_TRCO	[5]		0	Display TRCO on IRQ pin
	TUN_CAP	[3:0]		0000	Internal Tuning Capacitors (from 0 to 120pF in steps of 8pF)

Address	Register Name	Bit	Type	Default Value	Description
0x3A	TRCO_CALIB_DONE	[7]	R	0	Calibration of TRCO done (1=successful)
	TRCO_CALIB_NOK	[6]	R	0	Calibration of TRCO unsuccessful (1=not successful)
	Reserved	[5:0]	R	000000	Reserved
0x3B	SRCO_CALIB_DONE	[7]	R	0	Calibration of SRCO done (1=successful)
	SRCO_CALIB_NOK	[6]	R	0	Calibration of SRCO unsuccessful (1=not successful)
	Reserved	[5:0]	R	000000	Reserved

Serial Peripheral Interface (SPI)

This 4-wire standard SPI interface (Mode 1) can be used by the Microcontroller (µC) to program the AS3935. To enable the SPI as data interface, the Select Interface (SI) has to be set to low (GND).

The maximum clock operation frequency of the SPI is 2MHz.

Note(s): The clock operation frequency of the SPI should NOT be identical to the resonance frequency of the antenna (500kHz), in order to minimize the on board 500kHz noise.

Figure 24:
Serial Data Interface (SDI) Pins

Name	Signal	Signal Level	Description
CS	Digital Input	CMOS	Chip Select (Active Low)
MOSI	Digital Input	CMOS	Serial data input from the external unit to the ASxxxx
MISO	Digital Output	CMOS	Serial data output from the AS3935 to the external unit
SCLK	Digital Input	CMOS	Clock for serial data read and write

Note: MISO is set to tristate if CS is high. In this way more than one device can communicate on the same MISO bus.

SPI Command Structure

To activate the SPI the pin CS has to be pulled low. An SPI command consists of two bytes in series with the data being sampled on the falling edge of SCLK (CPHA=1). Figure 25 shows the command structure, starting from the MSB (B15) to the LSB (B0). This is also the sequence in which the command needs to be transmitted, MSB first down to LSB.

Figure 25:
Command Structure from MSB (B15) to LSB (B0)

MODE		Register Address / Direct Command						Register Data							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

The first two bits (B15 and B14) define the operating mode. There are two modes available – Read and Write/Direct command.

Figure 26:
Bits B15, B14

B15	B14	Mode
0	0	WRITE / DIRECT COMMAND
0	1	READ

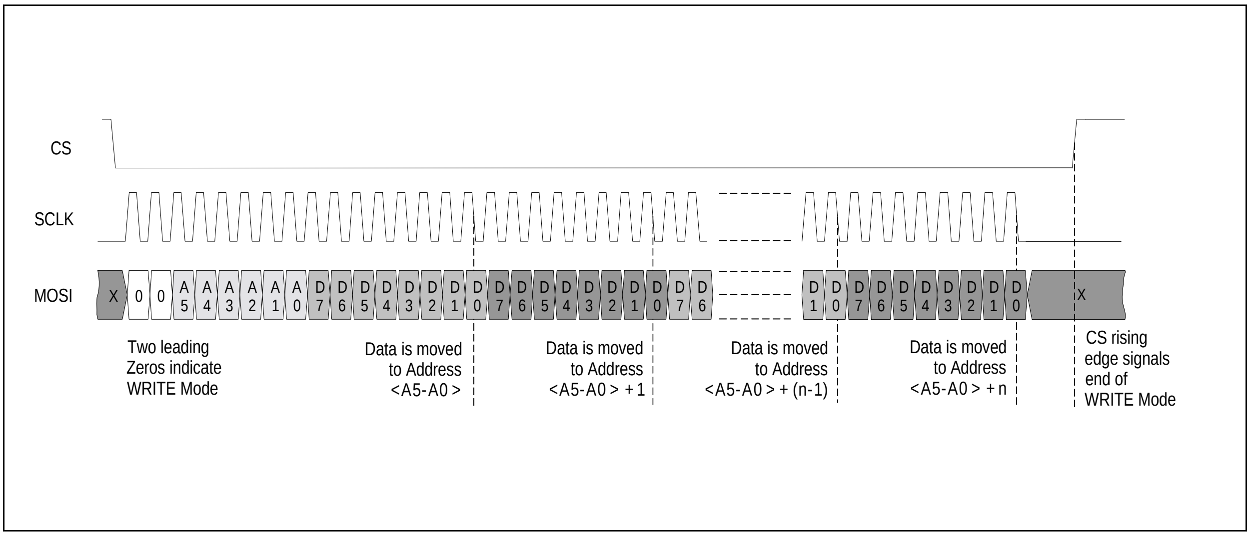
For read and write commands bits B13 to B9 define the register address that is to be read respectively written. The addresses assigned to the registers are shown in Figure 27. Direct commands are performed with a WRITE operation (see "Send Direct Command Byte" on page 23.

Figure 27:
Bits B13 to B9

B13	B12	B11	B10	B9	B8	Read / Write Register
0	0	0	0	0	0	0x00
0	0	0	0	0	1	0x01
0	0	0	0	1	0	0x02
0	0	0	0	1	1	0x03
0	0	0	1	0	0	0x04
0	0	0	1	0	1	0x05
0	0	0	1	1	0	0x06
0	0	0	1	1	1	0x07
…	…	…	…	…	…	…
…	…	…	…	…	…	…
1	1	1	0	1	0	0x3A
1	1	1	0	1	1	0x3B

Writing of Register Data

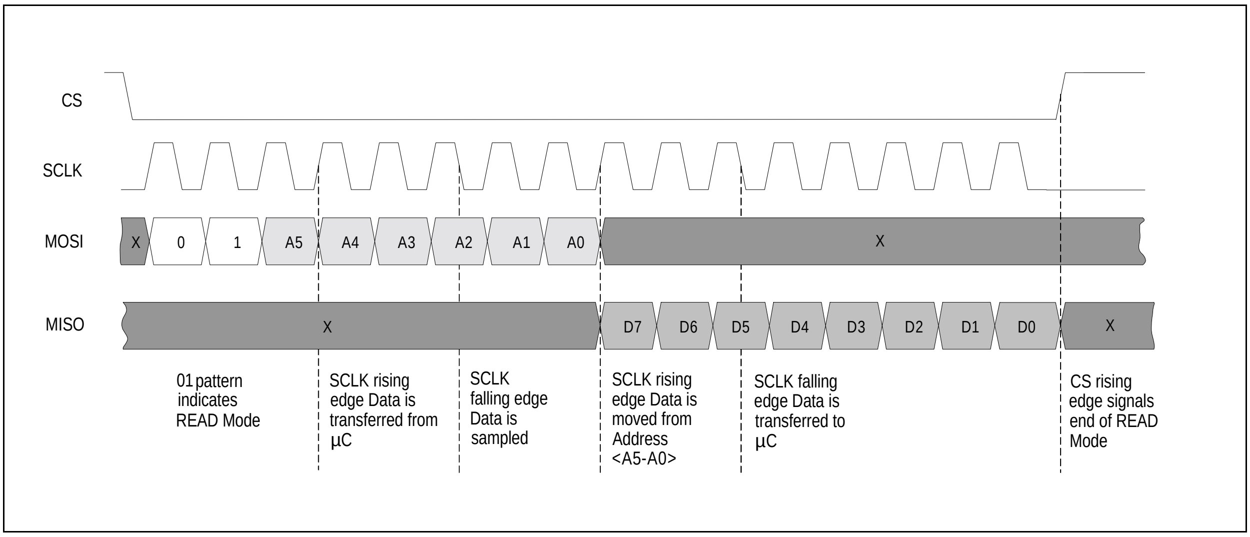
Figure 28:
SPI Page Write



Reading of Data from Addressable Registers (READ Mode)

After the register address has been transmitted on the MOSI signal, the data is sent from the AS3935 to the microcontroller via the MISO signal. At the end of the read session the signal CS needs to be toggled high-low-high to terminate the READ command. Thus the interface is ready for the next command. To transfer bytes from consecutive addresses the SPI master needs to keep the CS signal low and the SCLK active as long as the data needs to be read.

Figure 29:
SPI Read Byte



Send Direct Command Byte

It is possible to send direct commands by writing 0x96 in the registers **REG0x3C** and **REG0x3D**, as shown in the table below:

Figure 30:
Registers 0x3C, 0x3D

Direct Command	Register	Description
PRESET_DEFAULT	0x3C	Sets all registers in default mode
CALIB_RCO	0x3D	Calibrates automatically the internal RC Oscillators

I^2C

An I^2C slave interface is implemented for read/write access to the internal registers and to send direct commands. To enable the I^2C as interface, the Select Interface pin has to be set to the positive voltage supply (SI=VDD). The I2CL is the clock bus, while the I2CD is the data bus. An external pull-up resistor on the I2CL pin is needed.

The device addresses for the AS3935 in read or write mode are defined by:

0-0-0-0-0-a1-a0-0: write mode device address (DW)

0-0-0-0-0-a1-a0-1: read mode device address (DR)

Where a0 and a1 are defined by the pins 5 (ADD0) and 6 (ADD1). **The combination a0 = 0 (low) and a1 =0 (low) is explicitly not allowed for I^2C communication.**

Figure 31:
I^2C Timing Diagram

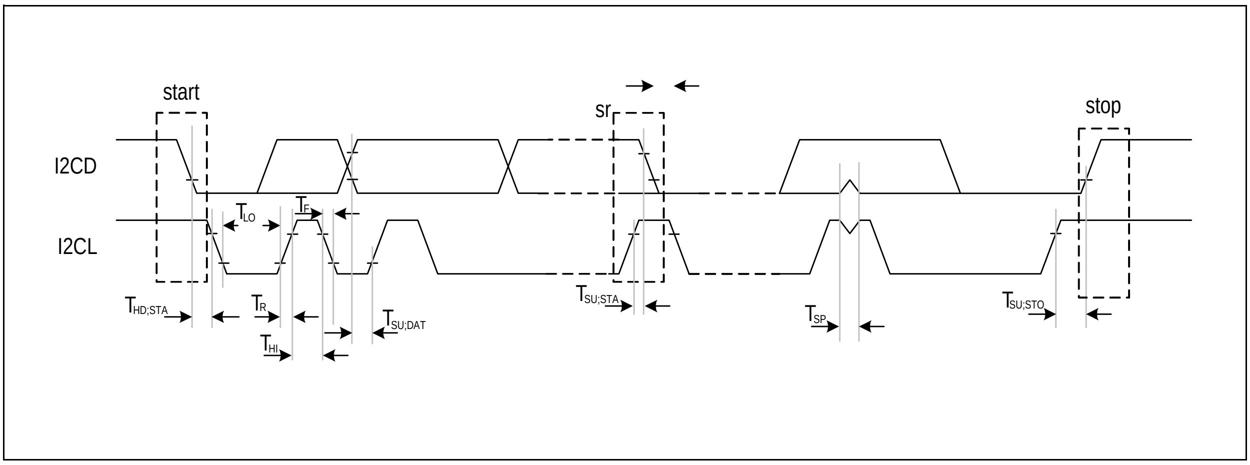


Figure 32:
I²C Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SP}	Spike intensity		50	100		ns
T_{HI}	High Clock Time	400 kHz Clock speed	330			ns
T_{LO}	Low Clock Time	400 kHz Clock speed	660			ns
T_{SU}		I2CD has to change Tsetup before rising edge I2CL	30			ns
T_{HD}		No hold time needed for I2CD relative to rising edge of I2CL	-40			ns
$T_{HD;STA}$	Within start condition, after low going I2CD, I2CL has to stay constant for specified hold time		300			ns
$T_{SU;STO}$	After high going edge of I2CL, I2CD has to stay constant for the specified setup time before STOP or repeated start condition is applied		100			ns
$T_{SU;STA}$	After high going edge of I2CL, I2CD has to stay constant for the specified setup time before STOP or repeated start condition is applied		100			ns

I²C Byte Write

The transmission begins with a START condition (S), which consists of a high-to-low transition of the I2CD bus when I2CL is high. The START condition is followed by the Device Write mode (DW), word address (WA: register address to write into) and the register data (reg_dat). Until the stop condition (P) the word address is automatically incremented at any register data.

Figure 33:
I²C Byte Write

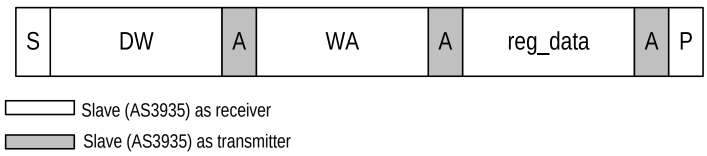


Figure 34:
I²C Page Write

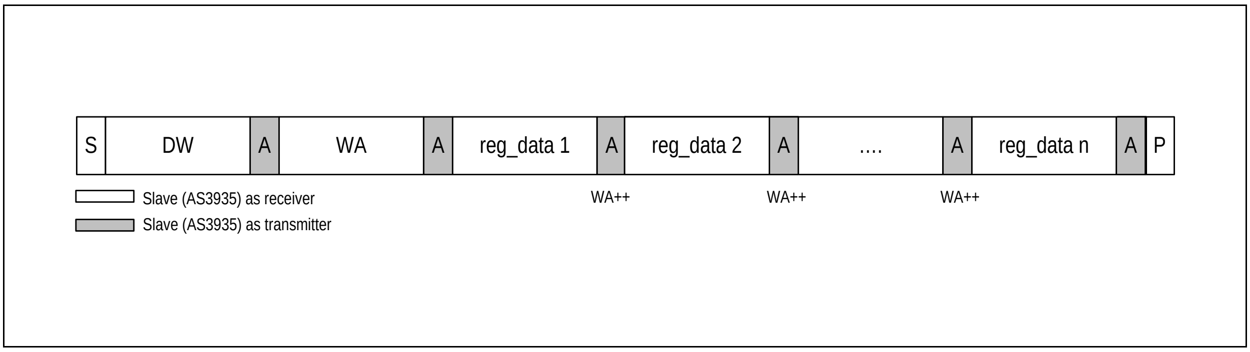


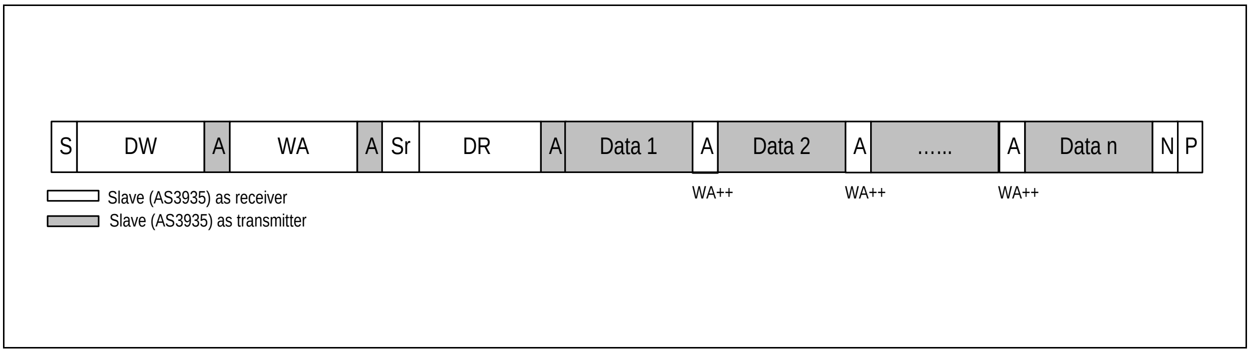
Figure 35:
I²C Abbreviations

Symbol	Description
S	START condition after STOP
Sr	Repeated START
DW	Device Address for write
DR	Device Address for read
WA	Word address
A	Acknowledge
N	No acknowledge
P	STOP condition
WA++	Internal address increment

I²C Register Read

To read data from the slave device, the master has to change the transfer direction. This can be done either with a Repeated START (Sr) condition followed by the device-read address (DR), or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode, any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 36:
I²C Page Read



Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction, a repeated START condition is issued on the 1st CLK pulse after the ACKNOWLEDGE bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state, the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a NOT ACKNOWLEDGE, and issues a STOP condition on the bus.

In contrast to the Random Read, in a sequential read the transferred register-data bytes are responded by an ACKNOWLEDGE from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission, the master has to send a NOT ACKNOWLEDGE following the last data byte and subsequently generate the STOP condition.

Direct Command

It is possible to send direct commands writing 0x96 in the registers **REG0x3C** and **REG0x3D**, as shown in the table below:

Figure 37:
Registers 0x3C, 0x3D

Direct Command	Register
PRESET_DEFAULT	0x3C
CALIB_RCO	0x3D

Voltage Regulator

The AS3935 can be supplied either by the internal voltage regulator or directly by an external supply.

Using the internal voltage regulator will increase the current consumption by around 5uA. To enable the internal voltage regulator the pins VDD and EN_VREG need to be connected to the supply voltage. A capacitance greater than 1uF needs to be connected at the pin VREG to ground to fulfill the stability requirements of the voltage regulator. The nominal regulated output voltage is 3V.

To supply the AS3935 directly by an external source (e.g. battery), the pin EN_VREG must be connected to ground. Both VDD and VREG then need to be connected to the supply voltage.

Analog Front-end (AFE) and Watchdog

The AFE amplifies and demodulates the AC-signal picked up by the antenna. The AS3935 is based on narrowband receiving techniques with a center frequency of 500 kHz and a bandwidth of about 33 kHz. The AFE gain can be considered as constant within the antenna's bandwidth. This is achieved by making the AFE bandwidth greater than the antenna bandwidth.

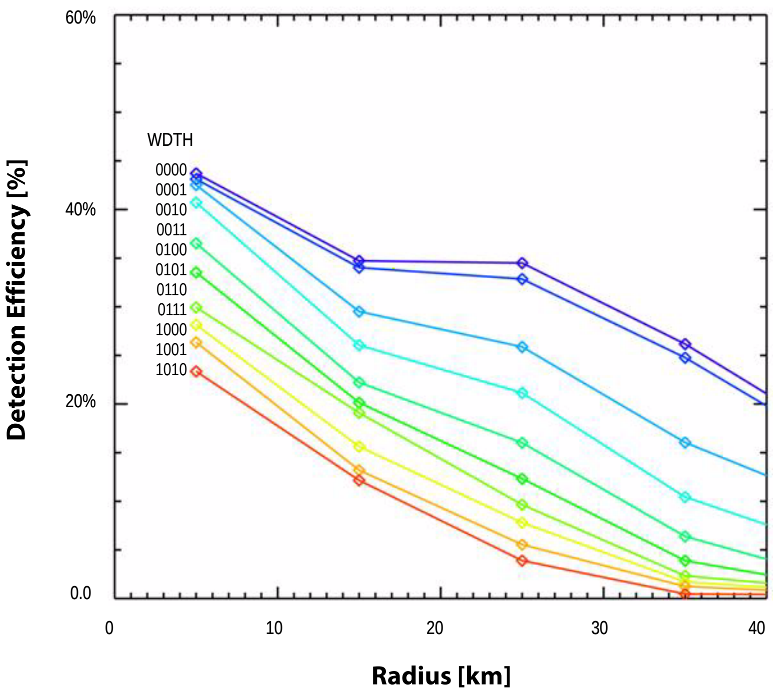
The AFE gain has been optimized for two operating environments as shown in Figure 38. By default the gain is set to Indoor. It is of paramount importance that the gain is set according to the surrounding environment, otherwise the sensor will not yield the desired results.

Figure 38:
AFE Setting, Outdoor vs. Indoor

AFE Setting	REG0x00[5:1]
Indoor	10010
Outdoor	01110

The output signal of the AFE is monitored by the watchdog. In case the signal crosses the watchdog threshold WDTH, the chip enters the Signal Verification mode (see Signal Verification on page 17). The level of this threshold can be set in **REG0x01[3:0]**. By increasing the threshold the AS3935 can be made more robust against disturbers. However, this will also make the sensor less sensitive for weaker signals from far away lightning events. In Figure 39 the degradation of the sensor's sensitivity towards lightning strike signals is shown as a function of distance at which the strikes occur for different WDTH settings.

Figure 39:
Detection Efficiencies vs. Distance for Different Settings for WDTH, if SREJ=0000



Noise Floor Generator and Evaluation

The output signal of the AFE is also used to generate the noise floor level. The noise floor is continuously compared to a reference voltage (noise threshold). Whenever the noise floor level crosses the noise threshold, the AS3935 issues an interrupt (INT_NH) to inform the external unit (e.g. MCU) that the AS3935 cannot operate properly due to the high input noise received by the antenna (e.g. blocker). It is possible to set the threshold for the noise floor limit with the bits **REG0x01[6:4]**, as defined in Figure 40.

Figure 40:
Settings for the Noise Floor Threshold

Continuous Input Noise Level [µVrms] (Outdoor)	Continuous Input Noise Level [µVrms] (Indoor)	REG0x01[6]	REG0x01[5]	REG0x01[4]
390	28	0	0	0
630	45	0	0	1
860	62	0	1	0
1100	78	0	1	1
1140	95	1	0	0
1570	112	1	0	1
1800	130	1	1	0
2000	146	1	1	1

INT_NH is displayed as long as the input noise level (blocker) is higher than the noise floor threshold. By default the setting **REG0x01[6:4]** =010 is used.

Lightning Algorithm

The lightning algorithm consists of hardwired logic. False events (man-made disturbers) which might trigger the AS3935 are rejected, while lightning events initiate calculations to estimate the distance to the head of the storm.

The Lightning algorithm is broken up into three sub blocks:

1. **Signal validation:** Verification that the incoming signal can be classified as lightning.
2. **Energy calculation:** Calculation of the energy of the single event.
3. **Statistical distance estimation:** According to the number of stored events (lightning), a distance estimate is calculated.

In case the incoming signal does not have the shape characteristic to lightning, the signal validation fails and the event is classified as disturber. In that case the energy calculation and statistical distance estimation are not performed and the sensor automatically goes back to listening mode.

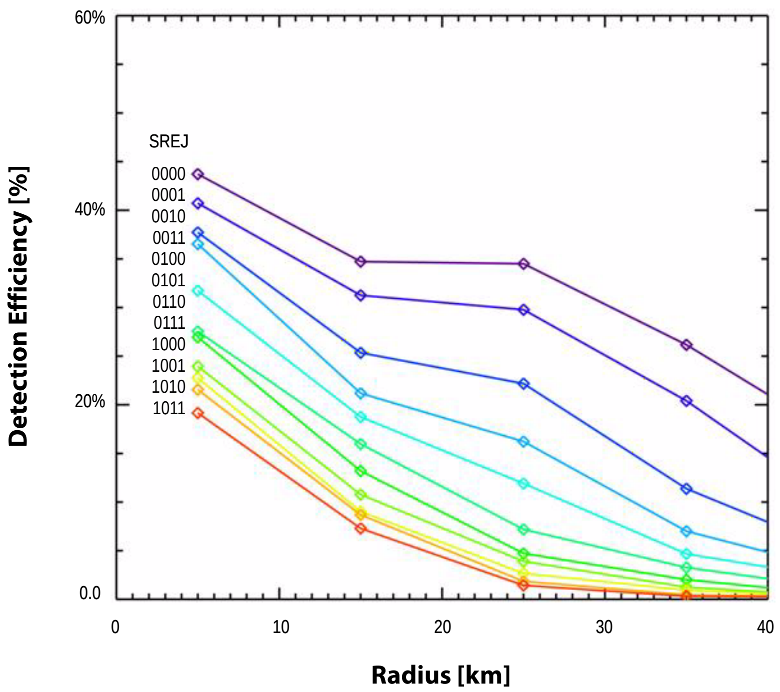
The shortest time span between two lightning strikes that the AS3935 can resolve is approximately one second.

Once a signal is classified as disturber the sensor is deactivated for a further 1.5s time period. As the duration of disturber signals can vary, this sensor down time will prevent the sensor from triggering repeatedly due to longer disturber events.

Signal Validation

During the signal validation phase the shape of the incoming signal is analyzed. The sensor can differentiate between signals that show the pattern characteristic of lightning strikes and man-made disturbers such as random impulses. Besides the watchdog threshold the spike rejection settings SREJ in **REG0x02[3:0]** can be used to increase the robustness against false alarms from such disturbers. By default the value is set to **REG0x02[3:0]** = 0010. Larger values in **REG0x02[3:0]** correspond to more robust disturber rejection, yet with the drawback of a decrease in detection efficiency. In Figure 41 the detection efficiency is illustrated as function of distance for various settings of SREJ.

Figure 41:
Detection Efficiencies vs. Distance for Different Setting of SREJ, if WDTH=0001



At the end of the signal verification, the AS3935 automatically returns to listening mode.

Energy Calculation

If the received signal is classified as lightning, the energy is calculated. The result of the energy calculation is then stored in the registers **REG0x06[4:0]**, **REG0x05[7:0]** and **REG0x04[7:0]**. This value is just a pure number and has no physical meaning.

Statistical Distance Estimation

The AS3935 generates an assessment of the estimated distance to the head of an approaching storm. This assessment is done based on statistical calculation. The statistical distance estimation block is where the estimated distance to the head of the storm is calculated. The output of the energy calculation block is stored along with timing information in an AS3935 internal memory. All of the events stored in the memory are then correlated with a look-up table to provide the distance estimate to the head of the storm. The algorithm automatically purges the memory of outdated data.

The estimated distance is output in **REG0x07[5:0]**. The conversion of the binary data to the respective distance in kilometer is given in Figure 42. The value in **REG0x07[5:0]** will change only if the statistical distance estimation yields a new estimated distance to the head of the storm, which can move closer or further away. The statistical distance estimation algorithm is hardwired and not accessible from the outside.

The estimated distance is directly represented in km in the register **REG0x07[5:0]** (binary encoded). The distance estimation can change also if no new event triggers the AS3935, as older events can be purged.

Figure 42:
Distance Estimation

REG0x07[5:0]	Distance [km]
111111	Out of range
101000	40
100101	37
100010	34
011111	31
011011	27
011000	24
010100	20
010001	17
001110	14
001100	12
001010	10
001000	8
000110	6

REG0x07[5:0]	Distance [km]
000101	5
000001	Storm is Overhead

The calculated energy is stored in registers **REG0x04[7:0]**, **REG0x05[7:0]** and **REG0x06[4:0]**.

Interrupt Management

Whenever events happen, the AS3935 pulls the IRQ high and displays the interrupt in the **REG0x03[3:0]**. Figure 43 shows the interrupt register. After the signal IRQ goes high the external unit should wait 2ms before reading the interrupt register. The interrupt bus IRQ is set back to low whenever the interrupt register is read out.

Figure 43:
Interrupts

Interrupt Name	REG0x03[3:0]	Description
INT_NH	0001	Noise level too high
INT_D	0100	Disturber detected
INT_L	1000	Lightning interrupt

The interrupt INT_NH is issued in case the noise level exceeds the threshold set with **REG0x01[6:4]** as described in the section Noise Floor Generator and Evaluation. INT_NH persists as long as the noise level is above the threshold.

The interrupt INT_D is displayed in case the signal validation classifies the signal as disturber event. It is possible to mask the interrupt INT_D by enabling the option MASK_DIST in **REG0x03[5]** (**REG0x03[5]** = 1). With MASK_DIST enabled, the signal on IRQ will not go high in case the signal is classified as disturber.

The AS3935 issues a lightning interrupt (INT_L) if a new event is detected. All new events are stored in the internal memory and build up a lightning statistic used by the distance estimation algorithm. If the AS3935 issues an interrupt and the Interrupt register is **REG0x03[3:0]** = 000 the distance estimation has changed due to purging of old events in the statistics, based on the lightning distance estimation algorithm.

In addition, it is possible to allow the AS3935 to issue lightning interrupts only if a minimum number of events (lightning) have been detected in the last 15 minutes. The minimum number of lightning events can be set with register **REG0x02[5:4]**.

Figure 44:
Minimum Number of Lightning Detection

Minimum Number of Lightning	REG0x02[5]	REG0x02[4]
1	0	0
5	0	1
9	1	0
16	1	1

When this feature is utilized a minimum number of lightning events must occur before the sensor triggers the lightning interrupt. Once the threshold is passed, the sensor will resume its normal interrupt handling. This eliminates false triggers by man-made disturbers that may pass the validation algorithm. It is possible to clear the statistics built up by the lightning distance estimation algorithm block by just toggling the bit **REG0x02[6]** (high-low-high).

Antenna Tuning

The AS3935 uses a loop antenna based on a parallel LC resonator. The antenna has to be designed to have its resonance frequency at 500kHz and a quality factor of around 15. By setting the register **REG0x08[7]** = 1 the antenna's resonance frequency is displayed on the IRQ pin as a digital signal. The external unit can measure this frequency and tune the antenna adding or removing the internal capacitors with the register **REG0x08[3:0]**. It is necessary to tune the antenna with an accuracy of ±3.5% to optimize the performance of the signal validation and distance estimation. The resonance frequency is internally divided by a factor, which is programmable with the register **REG0x03[7:6]**. Figure 45 shows the division ratio.

Figure 45:
Frequency Division Ratio for the Antenna Tuning

Division Ratio	REG0x03[7]	REG0x03[6]
16	0	0
32	0	1
64	1	0
128	1	1

Clock Generation

The clock generation is based on two different RC oscillators: a system RCO (SRCO) and a timer RCO (TRCO). The SRCO will run at about 1.1MHz and provides the main clock for the whole digital part. The TRCO is a low power low frequency oscillator and runs at 32.768 kHz. Frequency variations in these two oscillators, due to temperature change, are automatically compensated.

The output frequency of those oscillators can be displayed on the IRQ pin with register setting (**REG0x08[5]** =1 TRCO, while **REG0x08[6]** = 1 SRCO). Due to process variations, the frequency of both oscillators can be different from the nominal frequency. Therefore, it is possible to calibrate both with a direct command. The precision of the calibration will depend on the accuracy of the resonance frequency of the antenna. It is recommended to first trim the receiver antenna before the calibration of both oscillators is done.

REG0x3A[7:6] and **REG0x3B[7:6]** give information on the calibration status of the TRCO and SRCO oscillators, respectively. Once the calibration procedure has finished **REG0x3A[7]** for the TRCO (and **REG0x3B[7]** for the SRCO) will go high in case the calibration procedure was successful. In case a problem occurs during the calibration of the TRCO or SRCO, **REG0x3A[6]** (respectively **REG0x3B[6]**) will go high.

The result of calibration of the 2 oscillators is stored in a volatile memory and needs to be done every time after POR (e.g. battery change) but all oscillators are internally compensated in temperature and voltage supply variations.

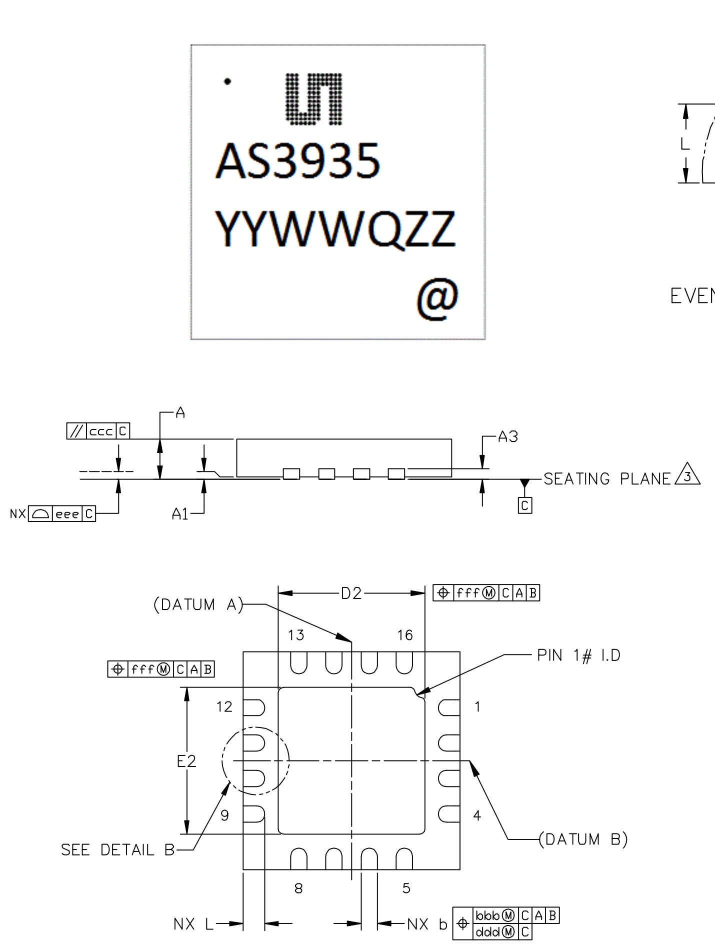
If the AS3935 is set in power-down mode, the TRCO needs to be recalibrated using the following procedure:

1. Send Direct command *CALIB_RCO*
2. Modify **REG0x08[6]** = 1
3. Wait 2ms
4. Modify **REG0x08[6]** = 0

Package Drawings & Markings

The device is available in a 16LD MLPQ (4x4mm) package.

Figure 46:
Drawings and Dimensions



Symbol	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF	
L	0.30	0.40	0.50
b	0.25	0.30	0.35
D		4.00 BSC	
E		4.00 BSC	
e		0.65 BSC	
D2	2.55	2.70	2.80
E2	2.55	2.70	2.80
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		16	

Note(s) and/or Footnote(s):

1. Dimensions & tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Figure 47:
Marking: YYWWQZZ

YY	WW	Q	ZZ	@
Year	Manufacturing Week	Plant identification letter	Traceability code	Sublot identifier

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RoHS: The term RoHS compliant means that ams products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

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Ordering & Contact Information

Figure 48:
Ordering Information

Ordering Code	Package Type	Marking	Delivery Form	Quantity
AS3935-BQFT	MLPQ 4x4 16LD	AS3935	7 inches Tape & Reel	1000 pcs

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