AN-143

Migrating to KSZ8051 Family PHY Transceivers

Introduction

This application note is written for Micrel customers who currently utilize the KSZ8041NL, KSZ8041MNL, or KSZ8041 MLL in their board designs.

Micrels KSZ8051 single-port 10/100 PHY transceivers leverage our industry-leading physical layer technology to reduce board real estate, conserve power, and reduce overall costs. Additional power saving features have been added to the KSZ8051. The KSZ8051 products provide a smooth migration path from existing KSZ8041 PHY transceivers.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

KSZ8051 Family

New and Revised KSZ8051 Family Features

The following are the features that have been added or changed in the KSZ8051 family, compared to the KSZ8041 family:

- Process technology changed to 0.13µm
- On-chip termination resistors for the differential pairs
- Power down and power saving modes, including Energy Detect Down, Power Down, and Slow Oscillator
- LinkMD® TDR-based cable diagnostics for identification of faulty copper cabling
- Parametric NAND Tree support for fault detection between chip I/Os and board
- Single 3.3V power supply with VDD I/O options for 1.8V, 2.5V, or 3.3V
- Built-in 1.2V regulator for core
- Unicast strap programmable.

KSZ8051 Applications

Some of the applications that are supported by the new features provided by the KSZ8051 family include the following:

- IP set-top box
- IP TV
- Game console
- IP phone
- Printer

The KSZ8051 family consists of five parts:

- KSZ8021RNL
- KSZ8031 RNL
- KSZ8051MNL
- KSZ8051RNL
- KSZ8051MLL
- KSZ8051FLL

Table 1 summarizes the primary functional differences between the members of the KSZ8051 family.

Part Number	Line	MAC	Package	Temp. Range	Description
KSZ8031RNL	10Base-T 100Base-TX LinkMD® Support	RMII	24-Pin QFN (4x4mm)	0˚C to 70˚C; -40˚C to +85˚C	C-temp; I-temp; Default: 25MHz in
KSZ8021RNL		RMII	24-Pin QFN (4x4mm)	0˚C to 70˚C; -40˚C to +85˚C	C-temp; I-temp; Default: 50MHz in
KSZ8051MNL		MII	32-Pin QFN (5x5mm)	0˚C to 70˚C; -40˚C to +85˚C	C-temp; I-temp
KSZ8051RNL		RMII	32-Pin QFN (5x5mm)	0˚C to 70˚C; -40˚C to +85˚C	C-temp; I-temp
KSZ8051MLL		MII	48-Pin LQFP (7x7mm)	0˚C to 70˚C; -40˚C to +85˚C	C-temp; I-temp
KSZ8051FLL	100Base-FX	MII	48-Pin LQFP (7x7mm)	0˚C to 70˚C; -40˚C to +85˚C	C-temp; I-temp

Table 1. KSZ8051 Family

Migration Summary

Table 1 summarizes the migration paths available from existing KSZ8041 products to the new KSZ8051 products.

Existing Part	Package	Interface	New Part	Package	Interface
N/A*			KSZ8021RNL	24QFN	RMII/10-100
N/A*			KSZ8031RNL	24QFN	RMII/10-100
KSZ8041NL	32MLF	MII/10-100	KSZ8051MNL	32QFN	MII/10-100
KSZ8041NL	32MLF	RMII/10-100	KSZ8051RNL	32QFN	RMII/10-100
KSZ8041RNL	32MLF	RMII/10-100	KSZ8051RNL	32QFN	RMII/10-100
KSZ8041MLL	48TQFP	MII/10-100	KSZ8051MLL	48LQFP	MII/10-100

Table 1. Migrating KSZ8041 to KSZ8051

*The KSZ8021NL and KSZ8031NL are functionally equivalent to the KSZ8051MNL, but there is no direct migration path because the packages and pin outs are different from previous products.

Functional Differences Between KSZ8041 and KSZ8051 Products

This section compares the features of the KSZ8041 and KSZ8051 family PHY transceivers.

Table 2 compares the power and package of the KSZ8041 and KSZ8051 family PHY transceivers.

Power and Package Comparison

Feature	KSZ8041NL KSZ8041RNL KSZ8041MLL	KSZ8051MNL KSZ8051RNL KSZ8051MLL	Benefits
Process Technology	0.18µm	0.13µm	Lower power consumption and reduced cost
VDDA (Analog Supply voltage)	3.3V	3.3V	
VDDIO (IO voltage)	3.3V	1.8, 2.5, 3.3V	Provides more flexibility for interfacing
Core Voltage	1.8V	1.2V	Lower power consumption and reduced cost
Package	32-pin MLF KSZ8041NL/RNL 48-pin TQFP KSZ8041MLL (only)	32-pin QFN KSZ8051MNL/RNL 48-pin LQFP KSZ8051MLL/FLL	
Temperature	Commercial, Industrial, Automotive	Commercial , Industrial, Automotive (future)	

Table 2. Power and Package Comparison

Table 3 compares the power management features of the KSZ8041 and KSZ8051 family PHY transceivers.

Power Management

Feature	KSZ8041NL KSZ8041RNL KSZ8041MLL	Power (8041NL) Including transformer	KSZ8051MNL KSZ8051RNL KSZ8051MLL	Power(8051MNL) Including transformer
Power Management (Software Control)	Programmable via MDC/MDIO bus		Programmable via MDC/MDIO bus	
100BT operation	Yes	98mA	yes	49mA
10BT operation	Yes	108mA	yes	39mA
Power Saving Mode	Yes	32mA	Yes	30mA
Energy Detect Power Down	No	NA	Yes	23mA
Power Down	No	4mA	Yes	2mA
Slow Oscillator + (Power Down)	No	NA	Yes (Lowest power down state)	8mA

Table 3. Power Management Comparison

Table 4 compares the line-side PHY layer features of the KSZ8041 and KSZ8051 family PHY transceivers.

PHY Layer Comparison

Feature	KSZ8041NL KSZ8041RNL 8041MLL	KSZ8051MNL KSZ8051RNL KSZ8051MLL	Benefits
On-Chip Termination	No	Yes	Added On-Chip Termination
Common mode voltages for TX/RX pairs	Same	Differential (RX is at 3.3V; TX is at 1.65V (~50% RX))	
Media Interfaces	MLL/NL/RNL/TL: 10/100BaseT FTL: 100BaseFX	MNL/RNL/MLL: 10/100BaseT FLL: 100BaseFX	

Table 4. PHY Layer Comparison—Line Side

Table 5 compares the MAC-side PHY layer features of the KSZ8041 and KSZ8051 family PHY transceivers.

Feature	KSZ8041NL KSZ8041RNL KSZ8041MLL	KSZ8051MNL KSZ8051RNL KSZ8051MLL	Benefits
Input Reference Clock	25MHz	25MHz	
RMII Clock Output	8041RNL Only	8051RNL Only	
MII back-to-back mode (Media Conversion, Repeater)	TL/FTL/MLL (only)	8051MLL/MNL/FLL (only)	
RMII back-to-back mode (Media Conversion, Repeater)	TL/FTL (only)	8051RNL/8031RNL/8021RNL	
MAC Interfaces	MII/RMII	MII/RMII	

Table 5. PHY Layer Comparison—MAC Side

Table 6 compares other PHY layer features of the KSZ8041 and KSZ8051 family PHY transceivers.

Feature	KSZ8041NL KSZ8041RNL KSZ8041MLL	KSZ8051MNL KSZ8051RNL KSZ8051MLL	Benefits
PHY Address 0	Broadcast (only)	Broadcast (default); Unicast (strap programmable)	Unicast strap programmable
NAND Tree	No	Yes	Added NAND Tree

Table 6. PHY Layer Comparison—Other

RMII Signal Diagram

The KSZ8051RNL RMII pin connections to the MAC are shown in the following figures for 25MHz Clock Mode and 50MHz Clock Mode.

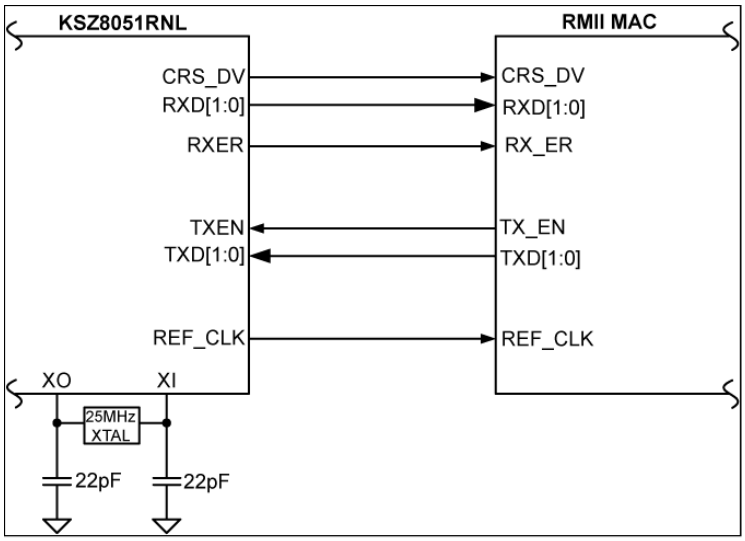

Figure 1. KSZ8051RNL RMII Interface (25MHz Clock Mode)

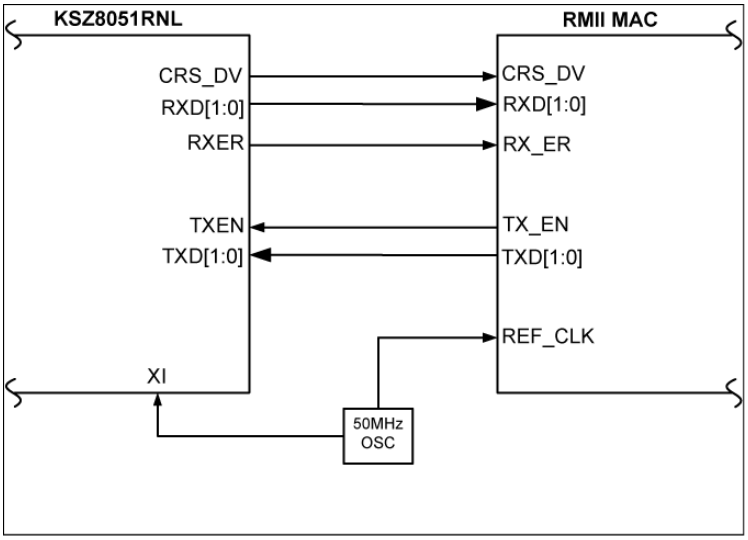

Figure 2. KSZ8051RNL RMII Interface (50MHz Clock Mode)

Schematic Differences

This section describes the schematic differences between the KSZ8041 and KSZ8051 families.

Figure 3 illustrates the copper port connections for the KSZ8041 family PHY transceivers.

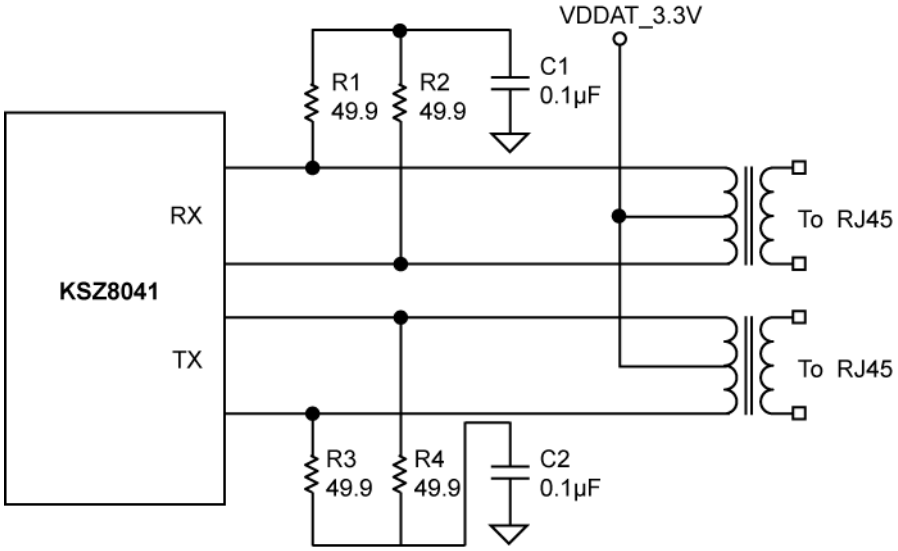

Figure 3. KSZ8041 Connection for Copper Ports

Figure 4 illustrates the copper port connections for the KSZ8051 family PHY transceivers.

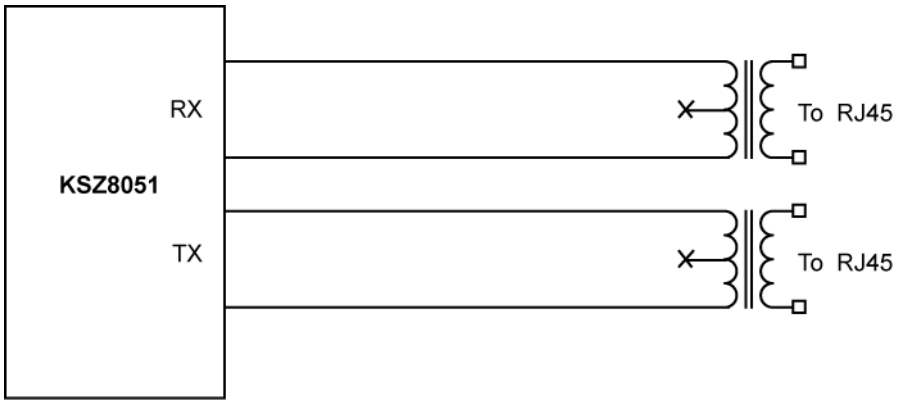

Figure 4. KSZ8051 Connection for Copper Ports

Figure 5 illustrates the capacitive (AC) coupling for the KSZ8041 family PHY transceivers.

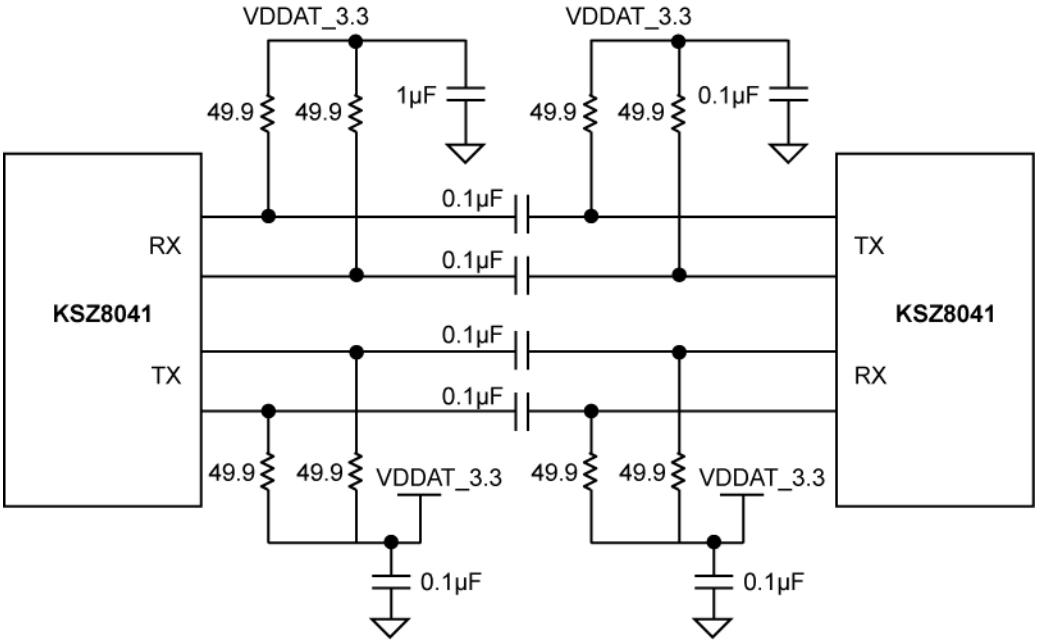

Figure 5. KSZ8041 Capacitive (AC) Coupling for Copper Ports

Figure 6 illustrates the capacitive (AC) coupling for the KSZ8051 family PHY transceivers.

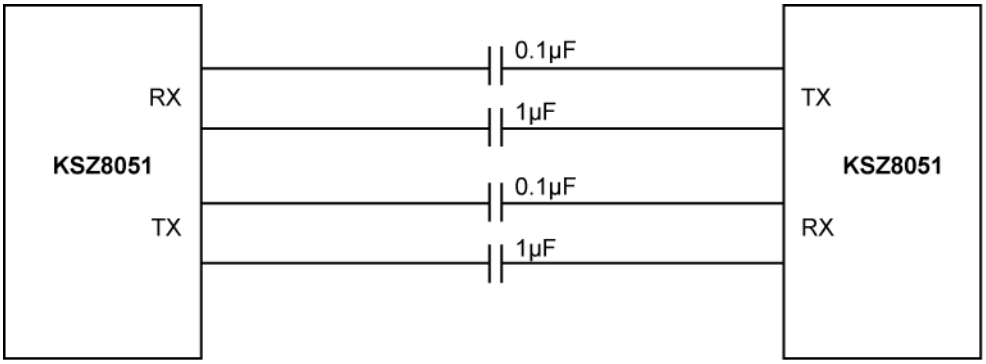

Figure 6. KSZ8051 Capacitive (AC) Coupling for Copper Ports

Register Differences Between KSZ0841NL/RNL/MLL and KSZ8051MNL/RNL/MLL

This section identifies the differences between the registers used by the KSZ8051 and KSZ8041 family PHY transceivers.

Register Map Differences Between KSZ8041NL/RNL/MLL and KSZ8051MNL/RNL/MLL

Table 7 lists the differences between the register maps for KSZ8041NL/RNL/MLL and KSZ8051MNL/RNL/MLL products. Where differences are not noted, the register maps are the same for both families of products.

KSZ8041NL/RNL/MLL		KSZ8051MNL/RNL/MLL	
Register	**Description**	**Register**	**Description**
00h	Basic Control	00h	Changes to power down definition and TX disable
11h	Reserved	11h	AFE Control 1
14h	MII Control	14h	Reserved
16h	Reserved	16h	Operation Mode Strap Override
17h	Reserved	17h	Operation Mode Strap Status
18h	Reserved	18h	Expanded Control
1Dh	Reserved (KSZ8041NL/RNL) LinkMD® Control/Status (KSZ8041MLL)	1Dh	LinkMD® Control/Status
1EH	Phy control 1	1EH	Phy control 1: register has been redefined, see below
1FH	Phy control 2	1FH	Phy control 2: register has been redefined, see below

Table 7. Changes to Register Map

Register 0h (Basic Control) Differences Between KSZ8041NL/RNL/MLL and KSZ8051MNL/RNL/MLL

Table 8 identifies the differences between the KSZ8041NL/RNL/MLL and KSZ8051MNL/RNL/MLL for Register 0h (Basic Control).

KSZ8041NL/RNL/MLL					KSZ8051MNL/RNL/MLL				
Register	**Name**	**Description**	**Mode**	**Default**	**Register**	**Name**	**Description**	**Mode**	**Default**
0.11	Power Down	1 = Power down mode 0 = Normal operation	RW	0	0.11	Power Down	1 = Power down mode 0 = Normal operation If software reset (register 0.15) is used to exit Power Down mode (register 0.11 = 1), two software reset writes (register 0.15 = 1) are required. First write clears Power Down mode; second write resets chip and re-latches the pin strapping pin values.	RW	0
0:0	Disable Transmit	0: enable 1: disable	RW	0	0:0	Reserved		RO	0

Table 8. Register 0h (Basic Control) Differences Between KSZ8041NL/RNL/MLL and KSZ8051MNL/RNL/MLL

Register 11h—Added for KSZ8051MNL/RNL/MLL

Table 9 lists the functions for Register 11h (AFE Control 1), which have been added to the KSZ8051MNL/RNL/MLL.

Address	Name	Description	Mode[1]	Default
Register 11h – AFE Control 1				
11.15:6	Reserved		RW	0000_0000_00
11.5	Slow Oscillator Mode Enable	Slow Oscillator Mode is used to disconnect the input reference crystal/clock on the XI pin and select the on-chip slow oscillator when the KSZ8051 device is not in use after power-up. 1 = Enable 0 = Disable This bit automatically sets software power down to the analog side when enabled.	RW	0
11.4:0	Reserved		RW	0_0000

Table 9. Register 11h (AFE Control 1) Added to KSZ8051MNL/RNL/MLL

Register 16h, 17h, and 18h—Added for KSZ8051MNL/RNL/MLL

Error! Reference source not found. lists the functions for Register 16h, 17h, and 18h, which have been added to the KSZ8051MNL/RNL/MLL.

Address	Name	Description	Mode[1]	Default
Register 16h – Operation Mode Strap Override				
16.15:11	Reserved		RW	0000_0
16.10	Reserved		RO	0
16.9	B-CAST_OFF override	1 = Override strap-in for B-CAST_OFF If bit is '1', PHY Address 0 is non-broadcast.	RW	0
16.8	Reserved		RW	0
16.7	MII B-to-B override	1 = Override strap-in for MII Back-to-Back mode (set also bit 0 of this register to 1) This bit is applicable for KSZ8051MNL only.	RW	0
16.6	RMII B-to-B override Reserved (KSZ8051MLL)	1 = Override strap-in for RMII Back-to-Back mode (set also bit 1 of this register to 1) This bit is applicable for KSZ8051RNL only.	RW	0
16.5	NAND Tree override	1 = Override strap-in for NAND Tree mode	RW	0
16.4:2	Reserved		RW	000
16.1	RMII override	1 = Override strap-in for RMII mode This bit is applicable for KSZ8051RNL only.	RW	0
16.0	MII override	1 = Override strap-in for MII mode This bit is applicable for KSZ8051MNL only.	RW	1

Address	Name	Description	Mode[1]	Default
Register 17h – Operation Mode Strap Status				
17.15:13	PHYAD[2:0] strap-in status	[000] = Strap to PHY Address 0 [001] = Strap to PHY Address 1 [010] = Strap to PHY Address 2 [011] = Strap to PHY Address 3 [100] = Strap to PHY Address 4 [101] = Strap to PHY Address 5 [110] = Strap to PHY Address 6 [111] = Strap to PHY Address 7	RO	
17.12:10	Reserved		RO	
17.9	B-CAST_OFF strap-in status	1 = Strap to B-CAST_OFF If bit is '1', PHY Address 0 is non-broadcast.	RO	
17.8	Reserved		RO	
17.7	MII B-to-B strap-in status	1 = Strap to MII Back-to-Back mode This bit is applicable for KSZ8051MNL only.	RO	
17.6	RMII B-to-B strap-in status Reserved (KSZ8051MLL)	1 = Strap to RMII Back-to-Back mode This bit is applicable for KSZ8051RNL only.	RO	
17.5	NAND Tree strap-in status	1 = Strap to NAND Tree mode	RO	
17.4:2	Reserved		RO	
17.4:1	Reserved	KSZ8051MLL only		
17.1	RMII strap-in status	1 = Strap to RMII mode This bit is applicable for KSZ8051RNL only.	RO	
17.0	MII strap-in status	1 = Strap to MII mode This bit is applicable for KSZ8051MNL only.	RO	
Register 18h – Expanded Control				
18.15:12	Reserved		RW	0000
18.11	EDPD Disabled	Energy Detect Power Down mode 1 = Disable 0 = Enable	RW	1
18.10	100Base-TX Preamble Restore	1 = Restore received preamble to MII output (random latency) 0 = Consume 1-byte preamble before sending frame to MII output for fixed latency This bit is applicable for KSZ8051MNL only.	RW	0
18.9:7	Reserved		RW	000
18.6	10Base-T Preamble Restore	1 = Restore received preamble to MII output 0 = Remove all 7-bytes of preamble before sending frame (starting with SFD) to MII output This bit is applicable for KSZ8051MNL only.	RW	0
18.5:0	Reserved		RW	00_0000

Table 10. Register 16h, 17h, and 18h Added to KSZ8051MNL/RNL/MLL

Register 1Dh—Added for KSZ8051MNL/RNL (exists in KSZ8041MLL and KSZ8051MLL)

Table 11 lists the functions for Register 1Dh , which has been added to the KSZ8051MNL/RNL.

Note: This register and its functions already exist for the KSZ8041MLL, except where noted.

Address	Name	Description	Mode[(1)]	Default
Register 1Dh – LinkMD® Control/Status				
1d.15	Cable Diagnostic Test Enable	1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared. 0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read.	RW/SC	0
1d.14:13	Cable Diagnostic Test Result	[00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test has failed	RO	00
1d.12:9	Reserved	Reserved in KSZ8041MLL		
1d.12	Short Cable Indicator	1 = Short cable (<10 meter) has been detected by LinkMD®. Completely new; not in KSZ8041MLL	RO	0
1d.11:9	Reserved		RW	000
1d.8:0	Cable Fault Counter	Distance to fault	RO	0_0000_0000

Table 11. Register 1Dh Added to KSZ8051MNL/RNL/MLL (already present in KSZ8041MLL except as noted)

Register 1Eh—Redefined for KSZ8051MNL/RNL/MLL

Table 12 lists the functions for Register 1Eh, which has been redefined for the KSZ8051MNL/RNL/MLL.

Address	Name	Description	Mode[(1)]	Default
Register 1Eh – PHY Control 1				
1e.15:10	Reserved		RO	0000_00
1e.9	Enable Pause (Flow Control)	1 = Flow control capable 0 = No flow control capability	RO	0
1e.8	Link Status	1 = Link is up 0 = Link is down	RO	0
1e.7	Polarity Status	1 = Polarity is reversed 0 = Polarity is not reversed	RO	
1e.6	Reserved		RO	0
1e.5	MDI/MDI-X State	1 = MDI-X 0 = MDI	RO	
1e.4	Energy Detect	1 = Presence of signal on receive differential pair 0 = No signal detected on receive differential pair	RO	0
1e.3	PHY Isolate	1 = PHY in isolate mode 0 = PHY in normal operation	RW	0

Address	Name	Description	Mode[1]	Default
1e.2:0	Operation Mode Indication	[000] = still in auto-negotiation [001] = 10Base-T half-duplex [010] = 100Base-TX half-duplex [011] = reserved [100] = reserved [101] = 10Base-T full-duplex [110] = 100Base-TX full-duplex [111] = reserved	RO	000

Table 12. Register 1Eh Added to KSZ8051MNL/RNL/MLL

Register 1Fh—PHY Control 2 has been redefined for KSZ8051MNL/RNL/MLL

Table 13 lists the new definition of Register 1Fh for the KSZ8051MNL/RNL/MLL.

Register 1Fh – PHY Control 2				
Address	**Name**	**Description**	**Mode[1]**	**Default**
1f.12	Reserved		RW	0
1f.7	RMII Reference Clock Select	1 = RMII 50MHz Clock Mode; clock input to XI (pin 9) is 50MHz 0 = RMII 25MHz Clock Mode; clock input to XI (pin 9) is 25MHz This bit is applicable for KSZ8051RNL only.	RW	0
1f.7.6	Reserved	KSZ8051MLL only		
1f.6	Reserved		RW	0
1f.5:4	LED mode	[00] =LED1 : Speed LED0 : Link/Activity [01] = LED1 : Activity LED0 : Link [10], [11] = Reserved	RW	00
1f.3	Disable Transmitter	1 = Disable transmitter 0 = Enable transmitter	RW	0
1f.2	Remote Loop-back	1 = Remote (analog) loop back is enable 0 = Normal mode	RW	0
1f.1	Enable SQE Test	1 = Enable SQE test 0 = Disable SQE test	RW	0
1f.0	Disable Data Scrambling	1 = Disable scrambler 0 = Enable scrambler	RW	0

Table 13. Register 1Fh Changes in KSZ8051MNL/RNL/MLL

Note:

1. RW = Read/Write.
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.
   LL = Latch low.

Pin Differences Between KSZ8041NL and KSZ8051MNL

This section provides information about pin changes that have occurred with the KSZ8051MNL.

Table 14 identifies the pin differences between the KSZ8041NL and the KSZ8051MNL. Changes are shown underlined. Pins that are not listed are the same for both products.

Pin Number	KSZ8041NL			KSZ8051MNL		
	Pin Name	**Type**	**Pin Function**	**Pin Name**	**Type**	**Pin Function**
2	VDDPLL_1.8	P	1.8V analog VDD	VDD_1.2	P	1.2V core VDD (power supplied by KSZ8051MNL) Decouple with 2.2µF and 0.1µF capacitors-to-ground.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7KΩ pull-up resistor.	MDIO	I/O	Management Interface (MII) Data I/O This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor.
17	VDDIO_3.3	P	3.3V digital VDD	VDDIO	P	3.3V, 2.5V or 1.8V digital VDD
19	RXC	O	MII Mode: Receive Clock Output	RXC / B-CAST_OFF	Ipd/O	MII Mode: MII Receive Clock Output Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. de-assertion of reset. See "Strapping Options" section for details.
21	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.	INTRP / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset. de-assertion of reset. See "Strapping Options" section for details.
22	TXC	O	MII Mode: Transmit Clock Output	TXC	I/O	MII Mode: MII Transmit Clock Output MII Back-to-Back Mode: MII Transmit Clock Input
30	LED0 / NWAYEN	Ipu/O	The LED0 pin is programmable via register 1Eh bits [15:14]	LED0 / NWAYEN	Ipu/O	The LED0 pin is programmable via register 1Fh bits [5:4]
31	LED1 / SPEED	Ipu/O	The LED1 pin is programmable via register 1Eh bits [15:14]	LED1 / SPEED	Ipu/O	The LED1 pin is programmable via register 1Fh bits [5:4]

Table 14. Pin Differences (KSZ8041NL and KSZ8051MNL)

Pin Differences Between KSZ8041RNL and KSZ8051RNL

This section provides information about pin changes for migrating board designs from the KSZ8041RNL to the KSZ8051RNL.

Table 15 identifies the pin differences between the KSZ8041RNL and the KSZ8051RNL. Changes are shown underlined. Pins that are not listed are the same for both products.

Pin Number	KSZ8041RNL			KSZ8051RNL		
	Pin Name	**Type**	**Pin Function**	**Pin Name**	**Type**	**Pin Function**
2	VDDPLL_1.8	P	1.8V analog VDD	VDD_1.2	P	1.2V core VDD (power supplied by KSZ8051MNL) Decouple with 2.2µF and 0.1µF capacitors to ground.
11	MDIO	I/O	Management Interface (MII) Data I/O This pin requires an external 4.7KΩ pull-up resistor.	MDIO	I/O	Management Interface (MII) Data I/O This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor.
17	VDDIO_3.3	P	3.3V digital VDD	VDDIO	P	3.3V, 2.5V or 1.8V digital VDD
19	REF_CLK	O	50MHz Clock Output This pin provides the 50MHz RMII reference clock output to the MAC.	REF_CLK / B-CAST_OFF	Ipd/O	RMII Mode: 25MHz Mode: This pin provides the 50MHz RMII reference clock output to the MAC. See also XI (pin 9). 50MHz Mode: This pin is a no connect. See also XI (pin 9). Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset. de-assertion of reset. See "Strapping Options" section for details.
21	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.	INTRP / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset. de-assertion of reset. See "Strapping Options" section for details.
26	NC	I	No connect	NC	I	No connect- It is recommended to tie this unused pin directly to ground.
27	NC	I	No connect	NC	I	No connect- It is recommended to tie this unused pin directly to ground.

Pin Number	KSZ8041RNL			KSZ8051RNL		
	Pin Name	**Type**	**Pin Function**	**Pin Name**	**Type**	**Pin Function**
30	LED0 / NWAYEN	Ipu/O	The LED0 pin is programmable via register 1Eh bits [15:14]	LED0 / NWAYEN	Ipu/O	The LED0 pin is programmable via register 1Fh bits [5:4]
31	LED1 / SPEED	Ipu/O	The LED1 pin is programmable via register 1Eh bits [15:14]	LED1 / SPEED	Ipu/O	The LED1 pin is programmable via register 1Fh bits [5:4]

Table 15. Pin Differences (KSZ8041RNL and KSZ8051RNL)

New Strapping Options with KSZ8051MNL/RNL

The KSZ8051MNL/RNL products provide the same strapping options as the KSZ8041NL/RNL. In addition, Table 16 describes the new strapping options available with the KSZ8051MNL/RNL.

Pin Number	Pin Name	Type(1)	Pin Function
19	B-CAST_OFF	Ipd/O	Broadcast Off – for PHY Address 0 Pull-up = PHY Address 0 is set as an unique PHY address Pull-down (default) = PHY Address 0 is set as a broadcast PHY address At the de-assertion of reset, this pin value is latched by the chip.
21	NAND_Tree#	Ipu/Opu	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable At the de-assertion of reset, this pin value is latched by the chip.

Table 16. New Strapping Options for KSZ8051MNL/RNL

Pin Differences Between KSZ8041MLL and KSZ8051MLL

This section provides information about pin changes that have occurred with the KSZ8051MNL.

Table 17 identifies the pin differences between the KSZ8041MLL and the KSZ8051MLL. Changes are shown underlined. Pins that are not listed are the same for both products.

Pin Number	KSZ8041MLL			KSZ8051MLL		
	Pin Name	**Type**	**Pin Function**	**Pin Name**	**Type**	**Pin Function**
4	VDDA_1.8	P	1.8V analog VDD	VDD_1.2	P	1.2V core VDD (power supplied by KSZ8051MLL) Decouple with 2.2µF and 0.1µF capacitors-to-ground, and join with pin 31 by power trace or plane.
5	VDDA_1.8	P	1.8V analog VDD	NC	-	No connect
6	V1.8_OUT	P	1.8V output voltage from chip	NC	-	No connect
8	VDDA_3.3	P	3.3V analog VDD	NC	-	No connect
25	VDDIO_3.3	P	3.3V digital VDD	VDDIO	P	3.3V, 2.5V or 1.8V digital VDD
26	VDDIO_3.3	P	3.3V digital VDD	NC	-	No connect

Pin Number	KSZ8041MLL			KSZ8051MLL		
	Pin Name	**Type**	**Pin Function**	**Pin Name**	**Type**	**Pin Function**
28	RXC	O	MII Mode: Receive Clock Output.	RXC / B-CAST_OFF	Ipd/O	MII Mode: MII Receive Clock Output Config Mode: The pull-up/pull-down value is latched as B-CAST_OFF at the de-assertion of reset.
31	VDD_1.8	P	1.8V digital VDD	VDD_1.2	P	1.2V core VDD (power supplied by KSZ8051MLL) Decouple with 0.1µF capacitor to ground, and join with pin 4 by power trace or plane.
32	INTRP	Opu	Interrupt Output: Programmable Interrupt Output Register 1Bh is the Interrupt Control/Status Register for programming the interrupt conditions and reading the interrupt status. Register 1Fh bit 9 sets the interrupt output to active low (default) or active high.	INTRP / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open-drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset.
42	LED0 / NWAYEN	Ipu/O	The LED0 pin is programmable via register 1Eh bits [15:14].	LED0 / NWAYEN	Ipu/O	The LED0 pin is programmable via register 1Fh bits [5:4].
43	LED1 / SPEED	Ipu/O	The LED1 pin is programmable via register 1Eh bits [15:14].	LED1 / SPEED	Ipu/O	The LED1 pin is programmable via register 1Fh bits [5:4].

Table 17. Pin Differences (KSZ8041MLL and KSZ8051MLL)

New Strapping Options with KSZ8051MLL

The KSZ8051MLL product provides the same strapping options as the KSZ8041MLL. In addition, Table 18 describes the new strapping options available with the KSZ8051MLL.

Pin Number	Pin Name	Type[1]	Pin Function
28	B-CAST_OFF	Ipd/O	Broadcast Off – for PHY Address 0 Pull-up = PHY Address 0 is set as an unique PHY address Pull-down (default) = PHY Address 0 is set as a broadcast PHY address At the de-assertion of reset, this pin value is latched by the chip.
32	NAND_Tree#	Ipu/Opu	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable At the de-assertion of reset, this pin value is latched by the chip.

Table 18. New Strapping Options for KSZ8051MLL

Description of Differences

Core Power 1.8 to 1.2V

The KSZ8051 uses 1.2V low core power for the low power consumption. Power is supplied by an internal LDO.

IO Power

The KSZ8051 support Digital IO power of 1.8, 2.5 or 3.3V. The KSZ8041 supports on 3.3V only.

Strapping Options

Pins 19 and 21 are new resistor strapping options on the 8051MNL/RNL. Pins 21 and 32 are the new strapping options for the 8051MLL. Details described above.

LDO (Internal 1.2V Regulator)

Pin 2 and 4 are the core power for the 8051MNL/RNL and 8051MLL respectively. Core power on the 8041 was 1..8V. It is 1.2V on the 8051.

REXT

100pf cap not needed for REXT on 8051.

Transformer

The quad transformer should be changed to part number H1664NL(Pulse). The internal center taps of RX and TX is must be disconnected.

On Chip Termination and Bias

KSZ8051 supports on-chip termination and internal biasing, so all external 49.9ohm termination resistors on the RX pair and TX pair must be removed. Do not connect the transformer center center tap to VDDAT. Just leave the center taps open or go through two capacitors to ground separately for RX and TX paths.

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Revision History

Revision	Date	Summary of Changes
0.1	9/1/10	Application note created.
1.0	12/6/10	Various fixes, added power comparison table