AN1709
APPLICATION NOTE

EMC DESIGN GUIDE
FOR ST MICROCONTROLLERS

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INTRODUCTION

The continuing demand for more performance, complexity and cost reduction require the semiconductor industry to develop Microcontrollers with both high density design technology and higher clock frequencies. This has intrinsically increased the noise emission and noise sensitivity. Application developers therefore, must now apply EMC "hardening" techniques in the design of firmware, PCB layout and at system level. This note aims to explain ST Microcontroller EMC features and compliance standards to help application designers reach the optimum level of EMC performance.

1.0

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1 EMC DEFINITIONS

1.1 EMC

ElectroMagnetic Compatibility (EMC) is the capability of a system to work properly, undisturbed by the electromagnetic phenomena present in its normal environment, and not to create electrical disturbances that would interfere with other equipment.

1.2 EMS

The ElectroMagnetic Susceptibility (EMS) level of a device is the resistance to electrical disturbances and conducted electrical noise. ElectroStatic Discharge (ESD) and Fast Transient Burst (FTB) tests determine the reliability level of a device operating in an undesirable electromagnetic environment.

1.3 EMI

The ElectroMagnetic Interference (EMI) is the level of conducted or radiated electrical noise sourced by the equipment. Conducted emission propagates along a cable or any interconnection line. Radiated emission propagates through free space.

2 EMC CHARACTERIZATION OF ST MICROCONTROLLERS

2.1 ELECTROMAGNETIC SUSCEPTIBILITY (EMS)

Two different type of tests are performed:

- Tests with device power-supplied (Functional EMS tests & Latch-up): The device behaviour is monitored during the stress.
- One test with device not powered supplied (Absolute Electrical Sensitivity): The device functionality and integrity is checked on tester after stress.

2.1.1 Functional EMS test

Functional Tests are performed to measure the robustness of ST Microcontrollers running in an application. Based on a simple program (toggling 2 LEDs through I/O ports), the product is stressed by 2 different EMC events until a run-away condition (failure) occurs.

2.1.1.1 Functional ElectroStatic Discharge Test (F_ESD Test)

This test is performed on any new microcontroller devices.Each pin is tested individually with a single positive or negative electrical discharge.This allows failures investigations inside the chip and further application recommendations to protect the concerned Microcontroller sensitive pins against ESD.

High static voltage has both natural and man made origins. Some specific equipment can reproduce this phenomenon in order to test the device under real conditions. Equipment, test sequence and standards are described here below.

ST Microcontroller F_ESD qualification test uses standards given in Table 1 as reference.

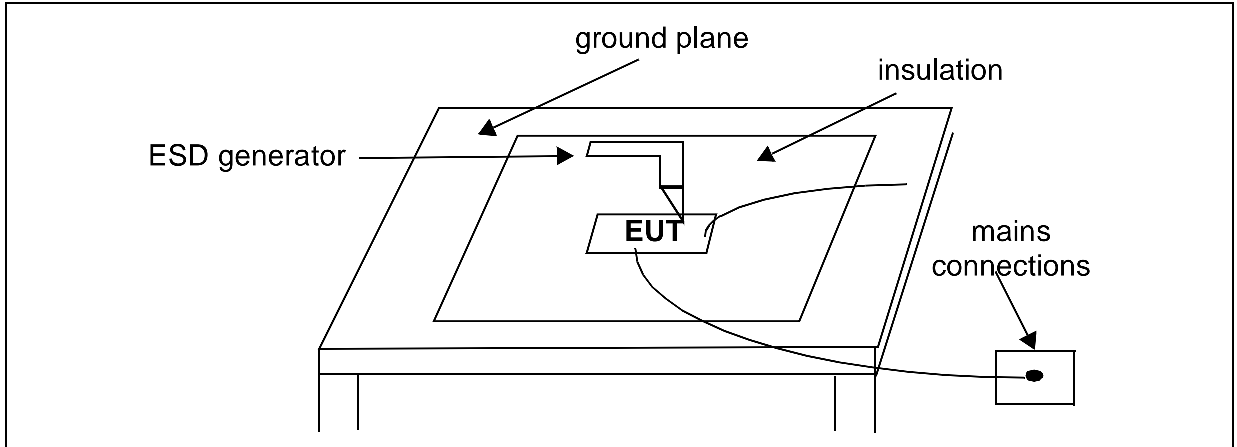
Table 1. ESD standards

EUROPEAN NORM	INTERNATIONAL NORM	DESCRIPTION
EN 61000-4-2	IEC 1000-4-2	Conducted ESD test

AEC-Q100-REUE is the Automotive controlling document.

F_ESD tests uses a signal source and a power amplifier to generate a high level field into The Microcontroller. The insulator is using a conical tip. This tip is placed on the Device or Equipment Under Test (DUT or EUT) and an electrostatic discharge is applied (see Figure 1.).

Figure 1. ESD test equipment



The equipment used to perform F_ESD test is a Generator NSG 435 (SCHAFFNER) compliant with the norm IEC 1000-4-2. The discharges are directly applied on each pin of the MCU.

Figure 2. Typical ESD Current Waveform in Contact-mode discharge

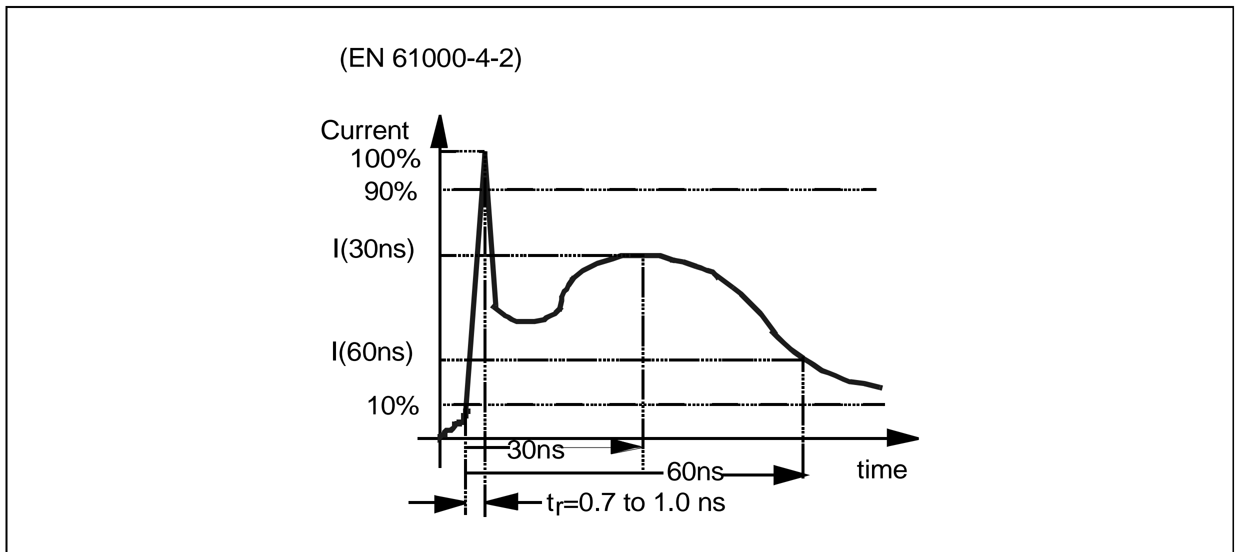
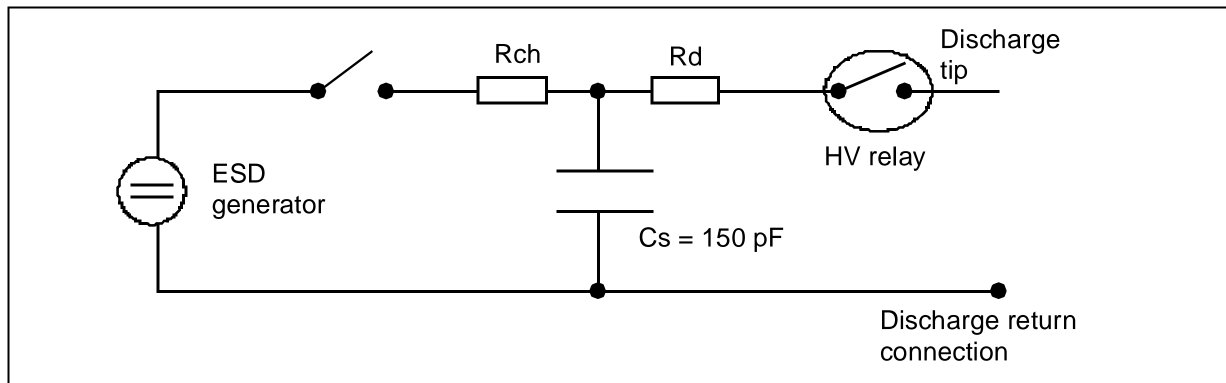


Figure 3. Simplified diagram of the ESD generator



(Rch = 50MΩ; Rd = 330Ω)

2.1.1.2 Fast Transient Burst (FTB)

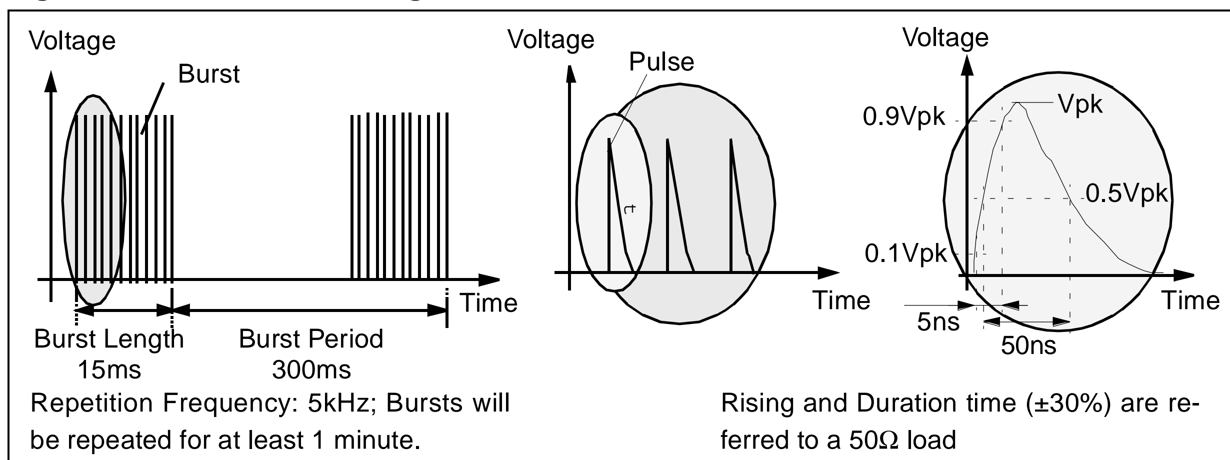
More complex than functional ESD, this test which submits the device to a large quantity of emitted disturbances in a short time, is useful for detecting infrequent and unrecoverable (Class B or C) Microcontroller states. FTB disturbances (see Figure 4.) are applied to the Microcontroller power lines through a capacitive coupling network.

ST Microcontroller FTB test correlates with the standards given in Table 2

Table 2. FTB standards

EUROPEAN NORM	INTERNATIONAL NORM	DESCRIPTION
EN61000-4-4	IEC 1000-4-4	Fast Transient Burst

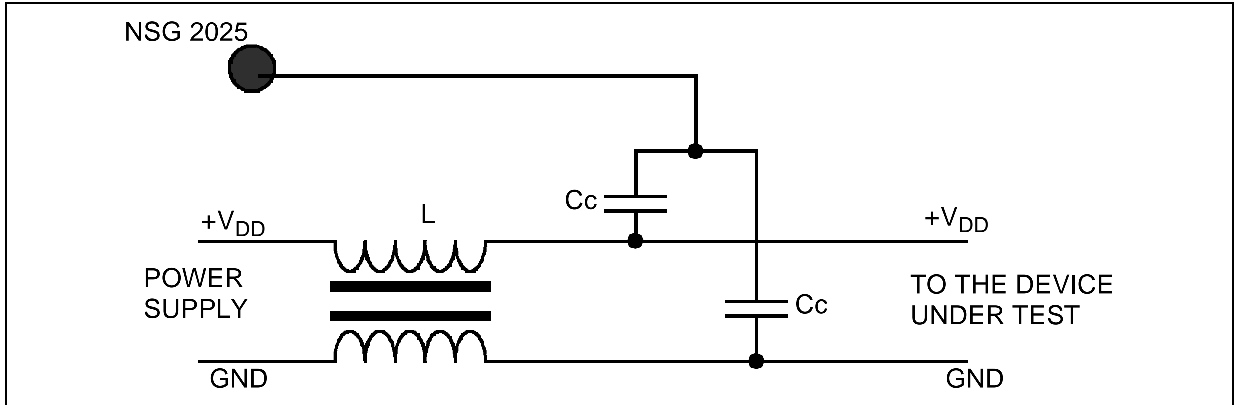
Figure 4. FTB Waveform Diagram



The spike frequency is 5 kHz. The generator produces bursts of spikes that last 15 ms every 300 ms (75 spikes).

The fast transients are coupled to the device DUT with capacitors C_C (See Figure 5.).

Figure 5. Coupling Network



Measurements are performed on a ground plane. The generator is connected to ground plane by a short wire. The supply wires are 10 cm from the ground plane. The DUT is on the insulator 10 cm from the ground plane. The FTB voltage level is increased until the device failure.

Severity Levels and Class help application designers to determine which ST microcontrollers are suitable for their target application, based on the susceptibility level (Severity level) and type of behavior (Class) indicated in the datasheet.

2.1.1.3 ST Severity Level & Behavior Class

The 1000-4-2 and 1000-4-4 standards do not refer specifically to semiconductor components such as microcontrollers. Usually electromagnetic stress is applied on other parts of the system such as connectors, mains, supplies... The energy level of the F_ESD and FTB test decreases before reaching the microcontroller, governed by the laws of physics. A large amount of statistical data collected by ST on the behaviour of MCUs in various application environments has been used to develop a correlation chart between ST F_ESD or FTB test voltage and 1000-4-2/1000-4-4 severity levels (See Table 3).

Table 3. ST ESD Severity levels

Severity Level	ESD (1000-4-2) Equipment standard (kV)	FTB (1000-4-4) Equipment standard (kV)	ST Testing Voltage ST internal EMC test (kV)
1	2	0.5	0-0.5
2	4	1	0.5-1
3	6	2	1-1.5
4	8	4	>1.5

In addition to this severity level, MCU behaviour under ESD stress can be grouped into different Behaviour Classes (See Table 4) according to EN 50082-2 norm:

Table 4. ST Behavior Classes

Class A	Class B	Class C	Class D
No failure detected	Failure detected but self recovery after disturbance	Needs an external user action to recover normal functionality	Normal functionality cannot be recovered

Any ST Microcontroller under the “acceptance limits” is rejected as a fail. The “target level” is the level used by ST to define good EMS performance.

Class B could be caused by:

– a parasitic reset correctly managed by the firmware (preferable case).

– deprogramming of a peripheral register or memory recovered by the application.

– a blocked status, recovered by a Watchdog or other firmware implementation.

Class C could be caused by:

– deprogramming of a peripheral register or memory not recovered by the application.

– a blocked application status requiring an external user action.

Table 5 shows ST target and acceptance limits.

Table 5. F_ESD / FTB target level & acceptance limit

	Acceptance limit	Target Level
F_ESD	0.5kV	>1kV
FTB	0.5kV	>1.5kV

Between “Acceptance limit” and “Target Level”, the device is relatively susceptible to noise. Special care during system design should be taken to avoid susceptibility issues.

Table 6 shows how F_ESD / FTB test results are presented in ST datasheets.

Table 6. Example of F_ESD / FTB test results

Symbol	Ratings	Conditions	Severity/Criteria
V_{F_ESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	T_A=+25°C	2/A, 3/B
V_{FTB}	Fast transient voltage burst limits to be applied through 100pF on VSS and VDD pins to induce a functional disturbance	T_A=+25°C	3/B

2.1.2 Latch-Up (LU)

2.1.2.1 Static Latch-Up (LU) test:

The Latch-up is a phenomenon which is defined by a high current consumption resulting from an overstress that triggers a parasitic thyristor structure and need a disconnection of the power supply to recover the initial state.

NOTES

1 The overstress can be a voltage or current surge, an excessive rate of change of current or voltage, or any other abnormal condition that causes the parasitic thyristor structure to become self-sustaining.

2 Latch-up will not damage the device if the current through the low-impedance path is sufficiently limited in magnitude or duration.

This test conforms to the EIA/JESD 78 IC latch-up standard.

True LU is self-sustaining and once triggered, the high current condition will remain until the power supply voltage is removed from the device. A temporary LU condition is considered to have been induced if the high current condition stops when only the trigger voltage is removed.

Two complementary static tests are required on 10 parts to assess the latch-up performance:

- **Power supply overvoltage** (applied to each power supply pin) simulates a user induced situation where a transient over-voltage is applied on the power supply.
- **Current injection** (applied to each input, output and configurable I/O pin) simulates an application induced situation where the applied voltage to a pin is greater than the maximum rated conditions, such as severe overshoot above V_{DD} or undershoot below ground on an input due to ringing.

Table 7 shows how LU test result is presented in ST datasheets.

Table 7. Example of the LU test result on ST72F521

Symbol	Parameter	Conditions	Class[1)]
LU	Static latch-up class	T_A=+25°C T_A=+85°C, T_A=+125°C (depending on the temperature range of the device)	A

1. Class description: “A” class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. “B” Class strictly covers all the JEDEC criteria (international standard).

2.1.2.2 Dynamic Latch-Up (DLU) test:

The product is evaluated for its LU susceptibility to ESD discharges when the microcontroller is “running.”

Increasing electrostatic discharges are supplied to every pin of the component until a Latch-up occurs. Result is the maximum tolerated voltage without Latch-up.

DLU Test methodology and characterization: Electro-Static Discharges (one positive then one negative test) are applied to each pin of 3 samples when the microcontroller is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the microcontroller and the component is put in reset mode.

Table 8 shows how the DLU test result is presented in ST datasheets.

Table 8. Example of DLU test Result on ST72F521

Symbol	Parameter	Conditions	Class[1)]
DLU	Dynamic latch-up class	V_{DD} =5V f_{OSC}=4MHz, T_A=+25°C	A

1. Class description: “A” class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. “B” Class strictly covers all the JEDEC criteria (international standard).

LU/DLU test equipment is same as the one used for the functional EMS (see Figure 1.).

2.1.3 Absolute Electrical Sensitivity

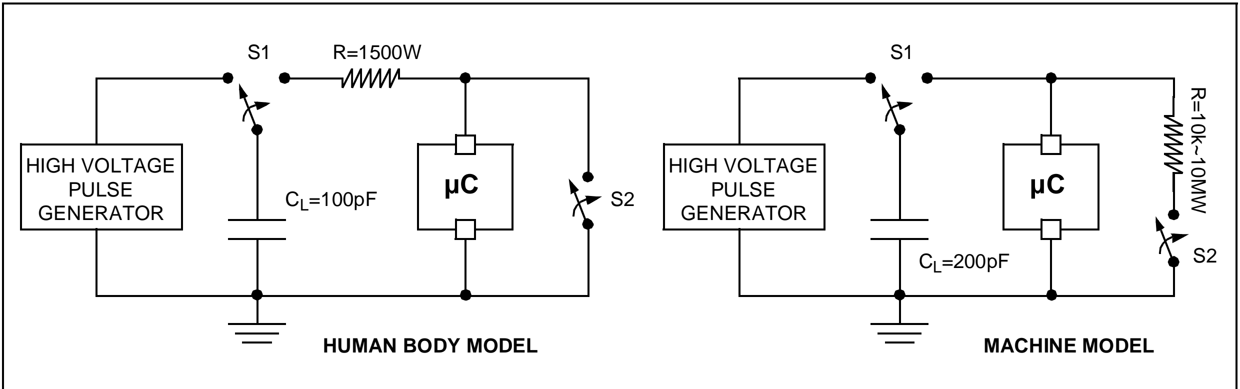
This test is performed to assess the components immunity against destruction caused by ESD.

Any devices that fails this electrical test program is classified as a failure.

Using automatic ESD tester, Electro-Static Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends of the number of supply pins of the device (3 parts*(n+1): n= supply pins). Two models are usually simulated: Human Body Model (HBM) and Machine Model (MM). All parts are re-tested on the production tester to verify the static and dynamic parameters still comply with the device datasheet (See Figure 6.).

This test conforms to the JESD22-A114A/A115A standard. See Figure 6. and the following test sequences.

Figure 6. Absolute Electrical Sensitivity test models



2.1.3.1 Human Body Model Test Sequence

The HBM ESD pulse simulates the direct transfer of electrostatic charge, from the Human Body, to a test device. A 100pF capacitor is discharged through a switching component and a 1.5 Kohm series resistor. This is currently the most requested industry model, for classifying device sensitivity to ESD.

– C_L is loaded through S1 by the HV pulse generator.

– S1 switches position from generator to R.

– A discharge from C_L through R (body resistance) to the µC occurs.

– S2 must be closed 10 to 100ms after the pulse delivery period to ensure the µC is not left in charge state. S2 must be opened at least 10ms prior to the delivery of the next pulse.

2.1.3.2 Machine Model Test Sequence

The MM ESD pulse emulates the rapid direct transfer of electrostatic charge, from a charged conductive object, such as a metallic tool or fixture, to a test device. This model consists of a discharged 200pF capacitor, with no series resistor. The demand for MM ESD testing has increased, with the replacement of individual packaging by automated systems.

– C_L is loaded through S1 by the HV pulse generator.

– S1 switches position from generator to the µC.

– A discharge from C_L to the µC occurs.

– S2 must be closed 10 to 100ms after the pulse delivery period to ensure the µC is not left in charge state. S2 must be opened at least 10ms prior to the delivery of the next pulse.

R (machine resistance), in series with S2, ensures a slow discharge of the µC.

Table 9 shows how HBM/MM ESD test results are presented in ST datasheets.

Table 9. Example of HBM/MM ESD test results on ST72F521

Symbol	Ratings	Conditions	Maximum value 1)	Unit
$V_{ESD(HBM)}$	Electro-static discharge voltage (Human Body Model)	T_A=+25°C	2000	V
$V_{ESD(MM)}$	Electro-static discharge voltage (Machine Model)	T_A=+25°C	200	

Notes:
1. Data based on characterization results, not tested in production.

2.2 ELECTROMAGNETIC INTERFERENCE (EMI)

2.2.1 EMI radiated test

This test correlates with the SAE J1752/3 standard.

This test gives a good evaluation of the contribution of the microcontroller to radiated noise in an application environment. It takes into account the MCU chip and also the package which has a major influence on the noise radiated by the device.

Below is the package EMI contribution from the highest to the lowest:

SDIP/DIP

SOP

QFP

TQFP

The test is performed in a Transverse Electromagnetic Mode Cell (TEMCELL) which allows radiated noise measurement in two directions, rotating the test board by 90°

Test description:

The firmware running is based on a simple application, toggling 2 LEDs through the I/O ports.

The main directives for an SAE PCB are (Figure 8.):
– 100 x 100mm square board
– At least 2-layer board (ideally 4-layer).
– 5mm conductive edges on both sides connected to ground for contact with TEMCELL.

Figure 7. shows a typical example of an MCU EMC test board schematics.

Figure 7. Example of test board schematics for ST7

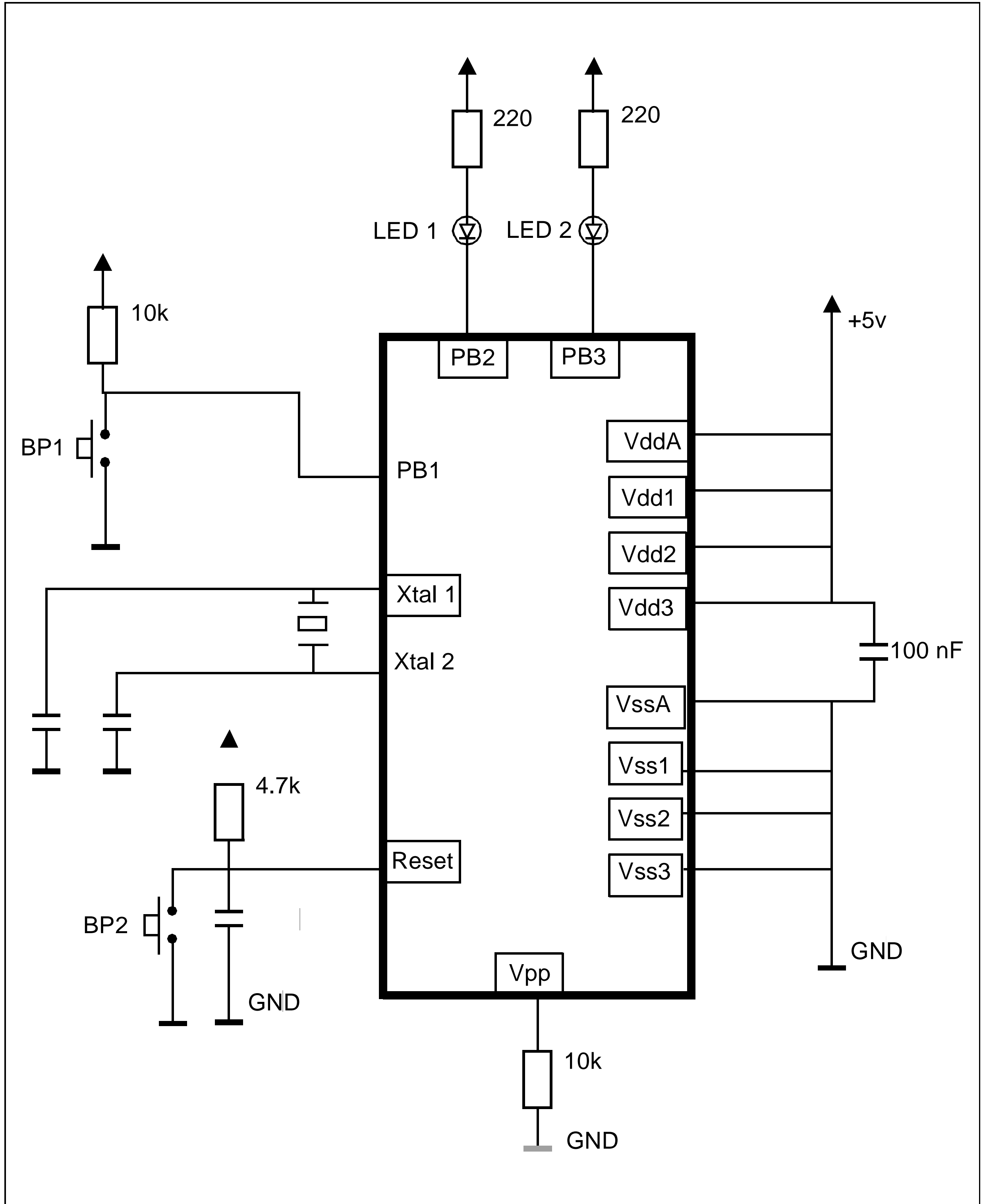
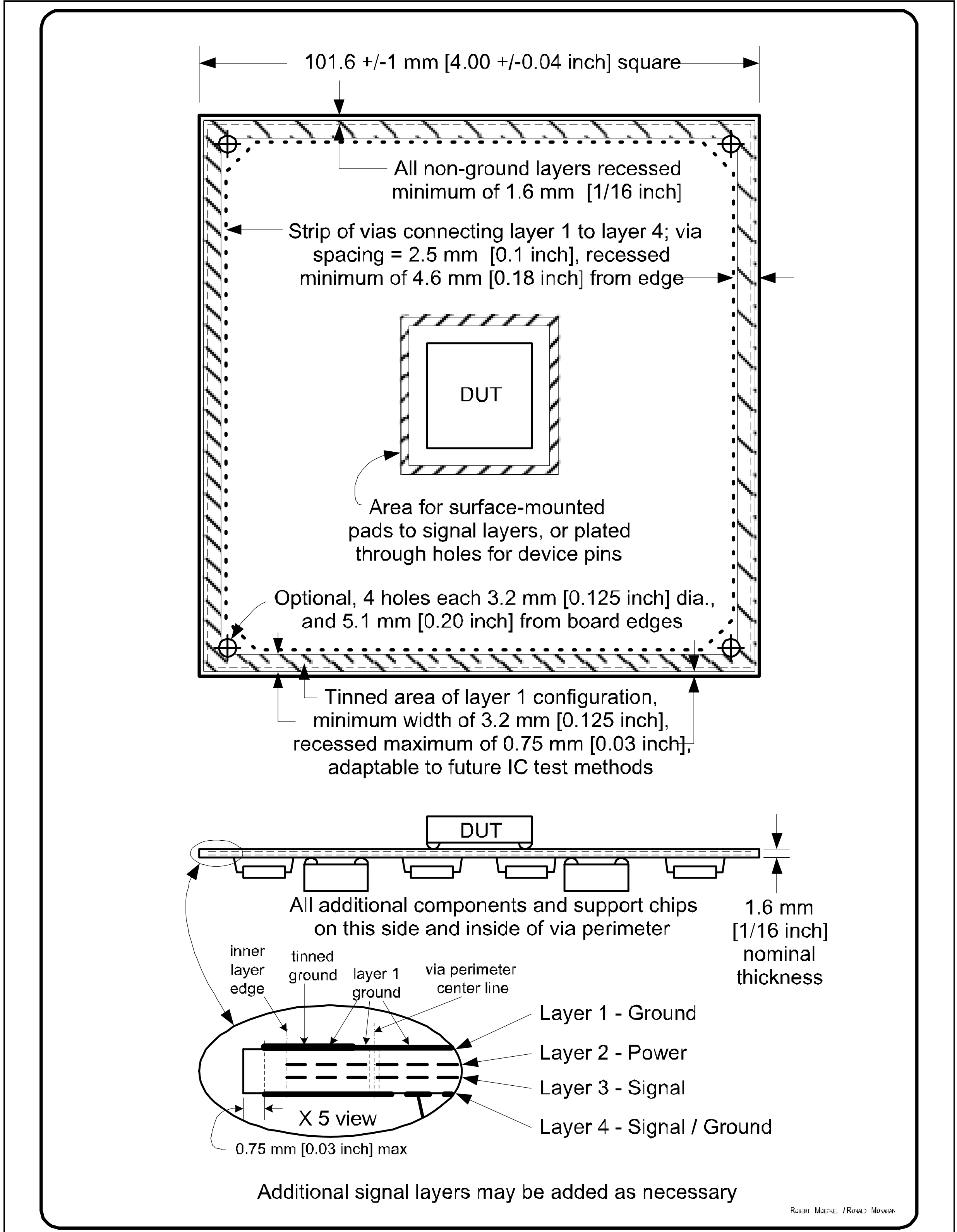


Figure 8. Test Printed Circuit Board specification according J1752/3 SAE standard

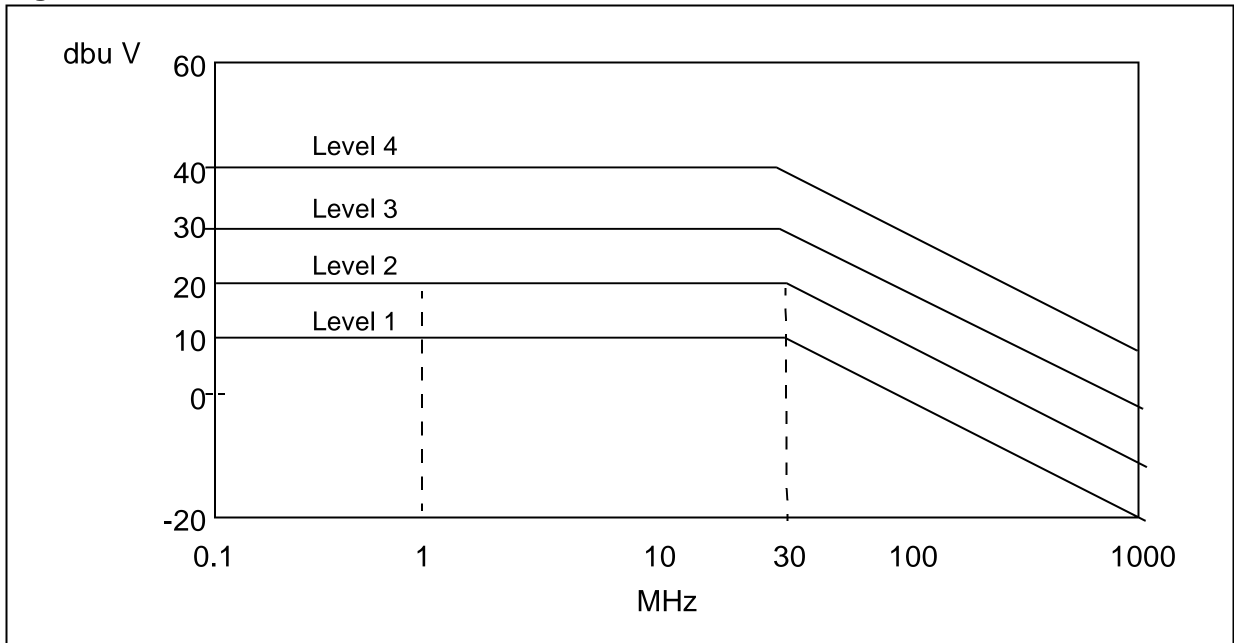


2.2.2 EMI level classification

The EMI classifications are directly based on the absolute frequency and amplitude of the emitted noise. Several international norms exist, based on different measurement methodologies, or emission levels, but the classification principle remains the same.

The standardized diagram (see Figure 9.) is useful to get a synthesis and a classification of EMI results, according to a standard framework. Each ST microcontroller EMI result is classified according to 4 SAE levels.

Figure 9. EMI level classification:



Below is the potential risk associated with each EMI level:

_ **higher than 4**. high risk due to EMI level.

_ **Level 4**. may require cost for EMI compliance.

_ **Level 3**. moderate EMI risk.

_ **Level 2**. minimal EMI risk.

Table 10 shows how EMI test results are presented in ST datasheets.

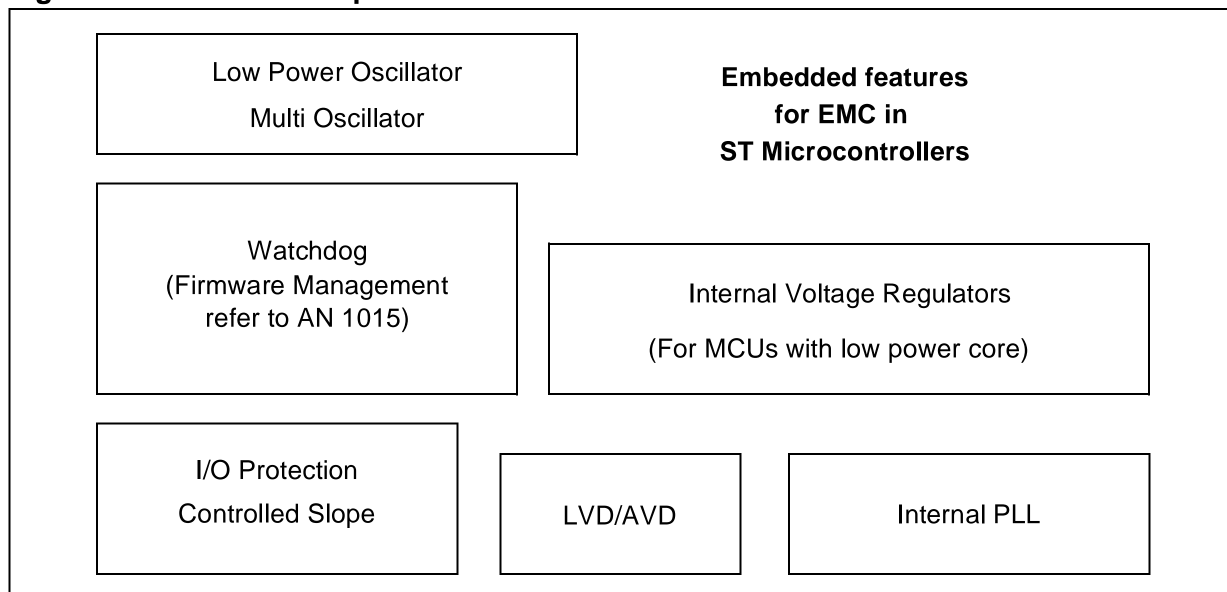
Table 10. Example of EMI results for ST72F521

To give a synthetic view of the emission spectrum, the highest emission level of 3 ranges of frequency is indicated. EMI data are provided with relevant information such as the device package and CPU frequency.

3 ST MCU DESIGN STRATEGY & EMC SPECIFIC FEATURE

At the initial specification of a new product, EMC dedicated features are implemented after an identification of EMC constraints imposed by the MCU target applications. You should refer to the specific product datasheet to know which of these feature described here are embedded.

Figure 10. Overview of specific features embedded in ST Microcontrollers



3.1 SUSCEPTIBILITY

3.1.1 Low Voltage Detector (LVD)

The purpose of the LVD is to ensure that the Microcontroller will always work in its safe operating area (see Figure 12.). In terms of EMS, the presence of the LVD makes the MCU more robust, ensuring that if any outside disturbance affects the power supply, the application can recover safely.

When V_{DD} is below the « Min Working V_{DD} » the behaviour of the Microcontroller is no longer guaranteed. There is not enough power to decode/execute the instructions and/or read the memory. When V_{DD} is below the LVD level the Microcontroller enters in reset state (internal reset High) in order to prevent unpredictable behaviour. There are 2 levels with 250mV hysteresis in order to avoid oscillating when the micro restarts. When a LVD reset occurs, a bit is set by HW. This bit can be used to recover an application.

The Low Voltage Detector function generates a static reset when the V_{DD} supply voltage is below a V_{IT-} reference value. This means that it secures the power-up as well as the power-down keeping the Microcontroller in reset.

The V_{IT-} reference value for a voltage drop is lower than the V_{IT+} reference value for power-on in order to avoid a parasitic reset when the MCU starts running and sinks current on the supply (hysteresis).

The LVD Reset circuitry generates a reset when V_{DD} is below:

– V_{IT+} when V_{DD} is rising
– V_{IT-} when V_{DD} is falling

The LVD function is illustrated in Figure 11..

The voltage threshold can be configured by option byte to be low, medium or high.

Provided the minimum V_{DD} value (guaranteed for the oscillator frequency) is above V_{IT-}, the MCU can only be in two modes:

– under full software control
– in static safe reset

In these conditions, secure operation is always ensured for the application without the need for external reset hardware.

During a Low Voltage Detector Reset, the $\overline{\text{RESET}}$ pin is held low, thus permitting the MCU to reset other devices.

Notes:

The LVD allows the device to be used without any external RESET circuitry.

The LVD is an optional function which can be selected by option byte. Refer to product specification.

Figure 11. Low Voltage Detector vs Reset

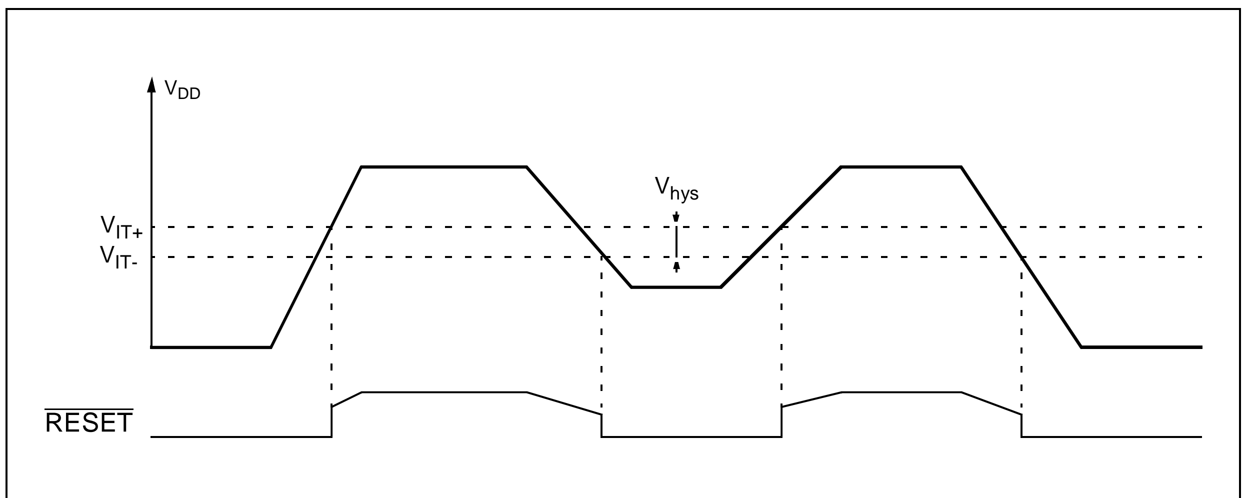
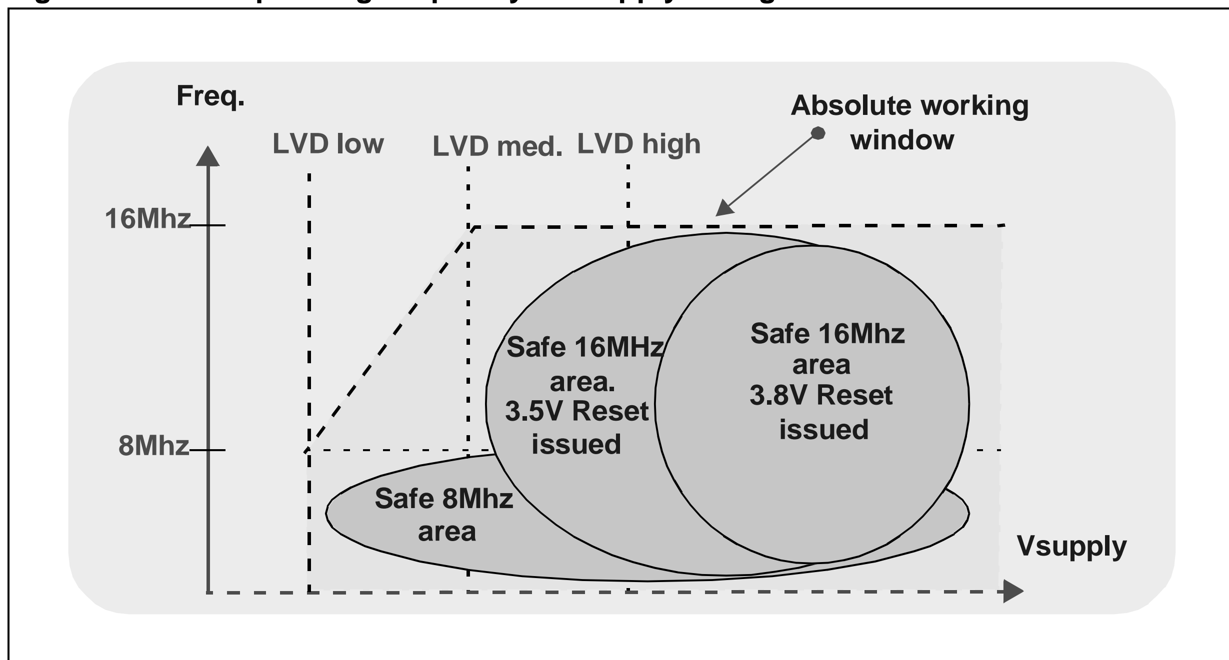


Figure 12. Max. Operating frequency vs. supply voltage.



The minimum value of each supply range is limited by the LVD threshold which can be configured at one of three levels (low, medium or high) depending on the application.

3.1.2 Auxiliary Voltage Detector (AVD)

Like the LVD, this feature improves EMS performance by ensuring that the microcontroller behaves safely when the power supply is disturbed by external noise.

The AVD feature can be used only if the LVD is activated. AVD has also different levels (around 200mV above LVD levels), enabling a early warning before the reset caused by the LVD. Then, when AVD threshold is crossed, an interrupt is generated, requesting for example some user action or preparing the application to shut down in the interrupt routine until the power supply returns to the correct level for the device (refer to the product datasheet).

Example: If f_{CPU} is between 8 MHZ and 16 MHZ the min. working level is 3.5 volt.

The Voltage Detector function (AVD) is based on an analog comparison between a V_{IT-} and V_{IT+} reference value and the V_{DD} main supply. The V_{IT-} reference value for falling voltage is lower than the V_{IT+} reference value for rising voltage in order to avoid parasitic detection (hysteresis).

The output of the AVD comparator is directly readable by the application software through a real time status bit (VDF). This bit is read only.

The AVD voltage threshold value is relative to the selected LVD threshold configured by option byte (see Microcontroller spec).

If the AVD interrupt is enabled, an interrupt is generated when the voltage crosses the $V_{IT+(AVD)}$ or $V_{IT-(AVD)}$ threshold (AVDF bit toggles).

In the case of a drop in voltage, the AVD interrupt acts as an early warning, allowing software to shut down safely before the LVD resets the microcontroller. (See Figure 13.).

The interrupt on the rising edge is used to inform the application that the V_{DD} warning state is over.

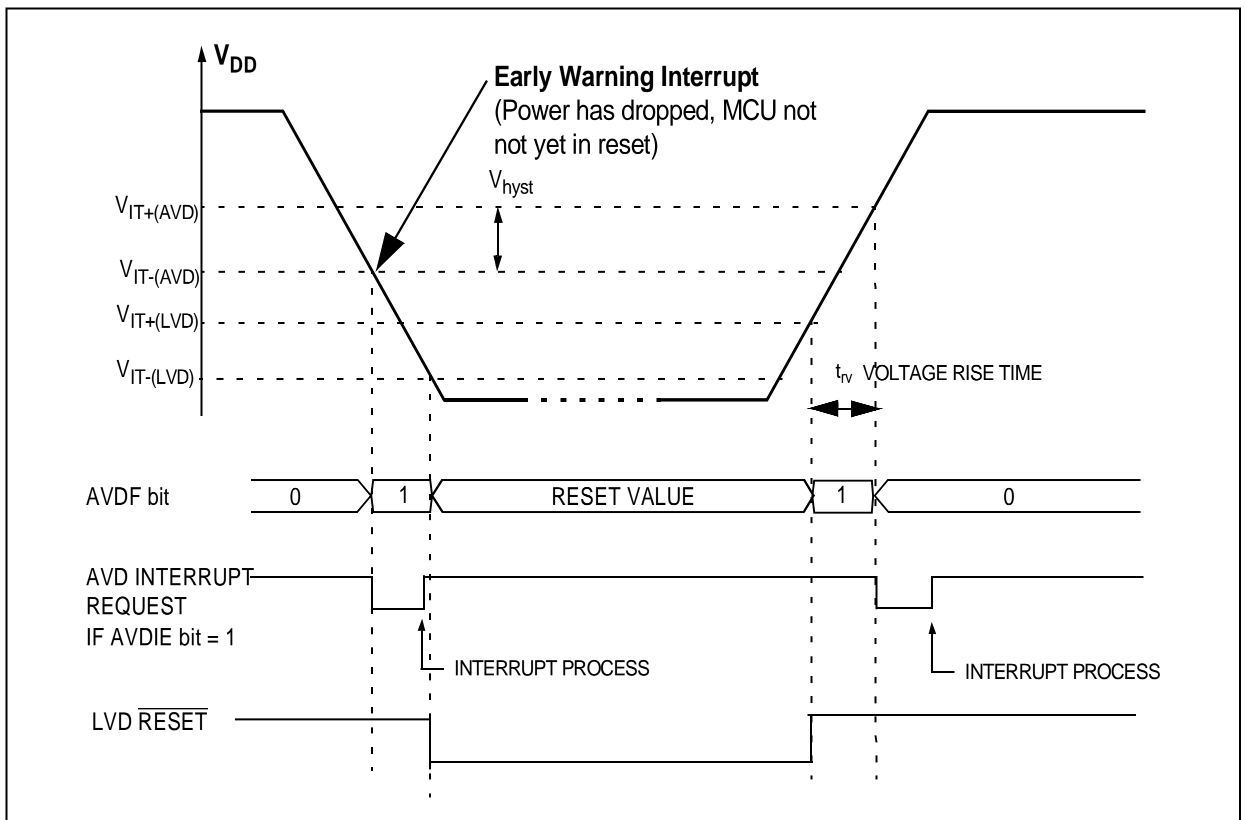
If the voltage rise time t_{rv} is less than 256 or 4096 CPU cycles (depending on the reset delay of the Microcontroller), no AVD interrupt will be generated when $V_{IT+(AVD)}$ is reached.

If t_{rv} is greater than 256 or 4096 cycles then:

– If the AVD interrupt is enabled before the $V_{IT+(AVD)}$ threshold is reached, then 2 AVD interrupts will be received: the first when the AVDIE bit is set, and the second when the threshold is reached.

– If the AVD interrupt is enabled after the $V_{IT+(AVD)}$ threshold is reached then only one AVD interrupt will occur.

Figure 13. Using the AVD to Monitor V_{DD}



3.1.3 I/O Features & properties

Although integrated circuit data sheets provide the user with conservative limits and conditions in order to prevent damage, sometimes it is useful for the hardware system designer to know the internal failure mechanisms: the risk of exposure to illegal voltages and conditions can be reduced by smart protection design.

It is not possible to classify and to predict all the possible damage resulting from violating maximum ratings and conditions, due to the large number of variables that come into play in defining the failures: in fact, when an overvoltage condition is applied, the effects on the device can vary significantly depending on lot-to-lot process variations, operating temperature, external interfacing of the Microcontroller with other devices, etc.

In the following sections, background technical information is given in order to help system designers to reduce risk of damage to the Microcontroller device.

3.1.3.1 Electrostatic Discharge and Latch-up

CMOS integrated circuits are generally sensitive to exposure to high voltage static electricity, which can induce permanent damage to the device: a typical failure is the breakdown of thin oxides, which causes high leakage current and sometimes shorts.

Latch-up is another typical phenomenon occurring in integrated circuits: unwanted turning on of parasitic bipolar structures, or silicon-controlled rectifiers (SCR), may overheat and rapidly destroy the device. These unintentional structures are composed of P and N regions which work as emitters, bases and collectors of parasitic bipolar transistors: the bulk resistance of the silicon in the wells and substrate act as resistors on the SCR structure. Applying voltages below V_{SS} or above V_{DD}, and when the level of current is able to generate a voltage drop across the SCR parasitic resistor, the SCR may be turned on; to turn off the SCR it is necessary to remove the power supply from the device.

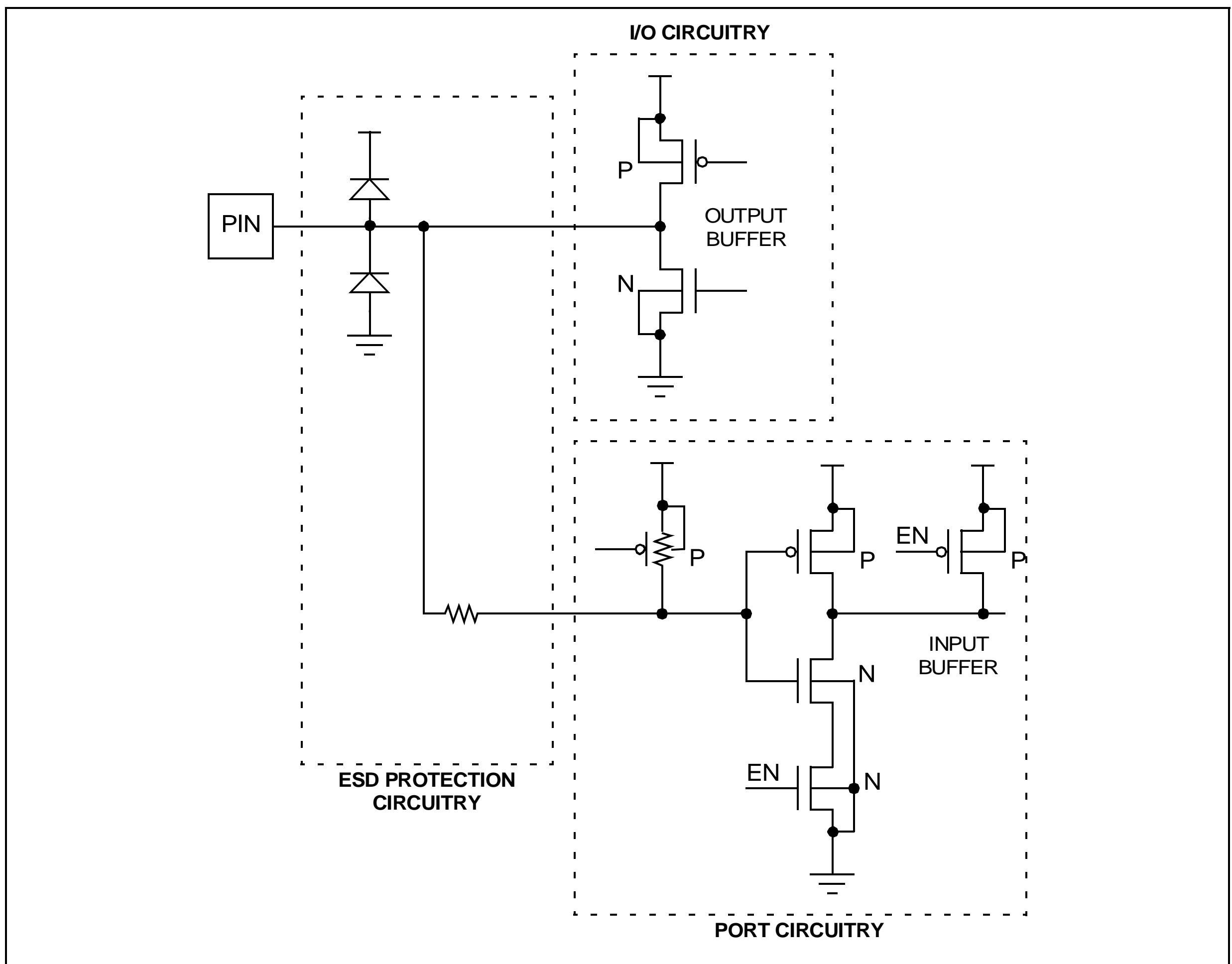
ST Microcontroller design implements layout and process solutions to decrease the effects of electrostatic discharges (ESD) and latch-up. Of course it is not possible to test all devices, due to the destructive nature of the mechanism; in order to guarantee product reliability, destructive tests are carried out on groups of devices, according to STMicroelectronics internal Quality Assurance standards and recommendations (see 2.1.2 Latch-Up (LU)).

3.1.3.2 Protective Interface

Although ST Microcontroller input/output circuitry has been designed taking ESD and Latch-up problems into account, for those applications and systems where ST Microcontroller pins are exposed to illegal voltages and high current injections, the user is strongly recommended to implement hardware solutions which reduce the risk of damage: low-pass filters and clamp diodes are usually sufficient in preventing stress conditions.

The risk of having out-of-range voltages and currents is greater for those signals coming from outside the system, where noise effect or uncontrolled spikes could occur with higher probability than for the internal signals; it must be underlined that in some cases, adoption of filters or other dedicated interface circuitries might affect global microcontroller performance, inducing undesired timing delays, and impacting the global system speed.

Figure 14. Digital Input/Output - Push-Pull



3.1.3.3 Internal Circuitry: Digital I/O pin

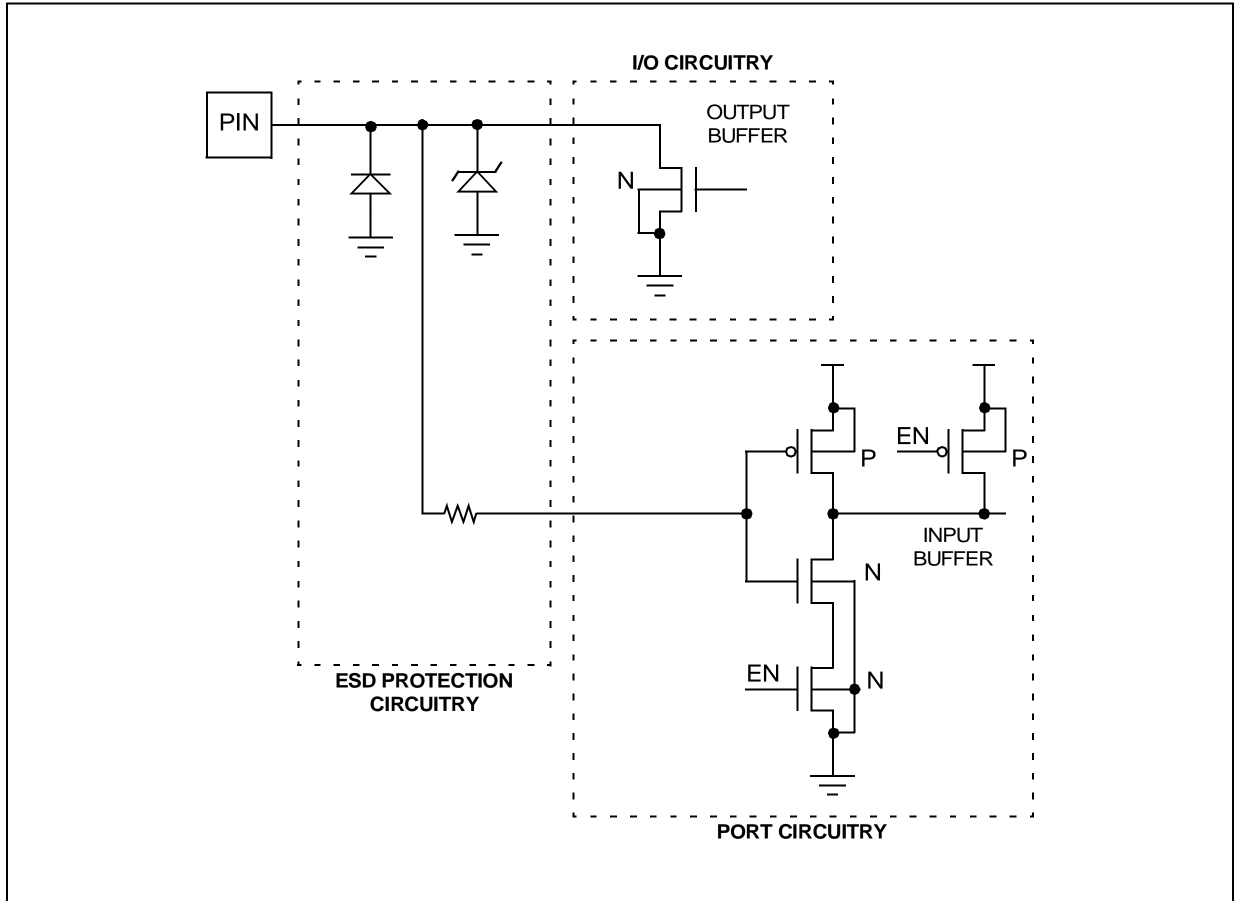
Figure 14. shows a schematic representation of an ST Microcontroller pin able to operate either as an input or as an output is shown. The circuitry implements a standard input buffer and a push-pull configuration for the output buffer. It is evident that although it is possible to disable the output buffer when the input section is used, the MOS transistors of the buffer itself can still affect the behaviour of the pin when exposed to illegal conditions. In fact, the P-channel transistor of the output buffer implements a direct diode to V_{DD} (P-diffusion of the drain connected to the pin and N-well connected to V_{DD}), while the N-channel of the output buffer implements a diode to V_{SS} (P-substrate connected to VSS and N-diffusion of the drain connected to the pin). In parallel to these diodes, dedicated circuitry is implemented to protect the logic from ESD events (MOS, diodes and input series resistor).

The most important characteristic of these extra devices is that they must not disturb normal operating modes, while acting during exposure to over limit conditions, avoiding permanent damage to the logic circuitry.

According to the MCU used, some I/O pins can be programmed to work also as open-drain outputs, by simply writing in the corresponding register of the I/O Port. The gate of the P-channel of the output buffer is disabled: it is important to highlight that physically the P-channel transistor is still present, so the diode to V_{DD} works. In some applications it can occur that the voltage applied to the pin is higher than the V_{DD} value (supposing the external line is kept high, while the Microcontroller power supply is turned off): this condition will inject current through the diode, risking permanent damages to the device.

In any case, programming I/O pins as open-drain can help when several pins in the system are tied to the same point: of course software must pay attention to program only one of them as output at any time, to avoid output driver contentions; it is advisable to configure these pins as output open-drain in order to reduce the risk of current contentions.

Figure 15. Digital Input/Output - True Open Drain Output



In Figure 15. a true open-drain pin schematic is shown. In this case all paths to V_{DD} are removed (P-channel driver, ESD protection diode, internal weak pull-up) in order to allow the system to turn off the power supply of the microcontroller and keep the voltage level at the pin high without injecting current in the device. This is a typical condition which can occur when several devices interface a serial bus: if one device is not involved in the communication, it can be disabled by turning off its power supply to reduce the system current consumption.

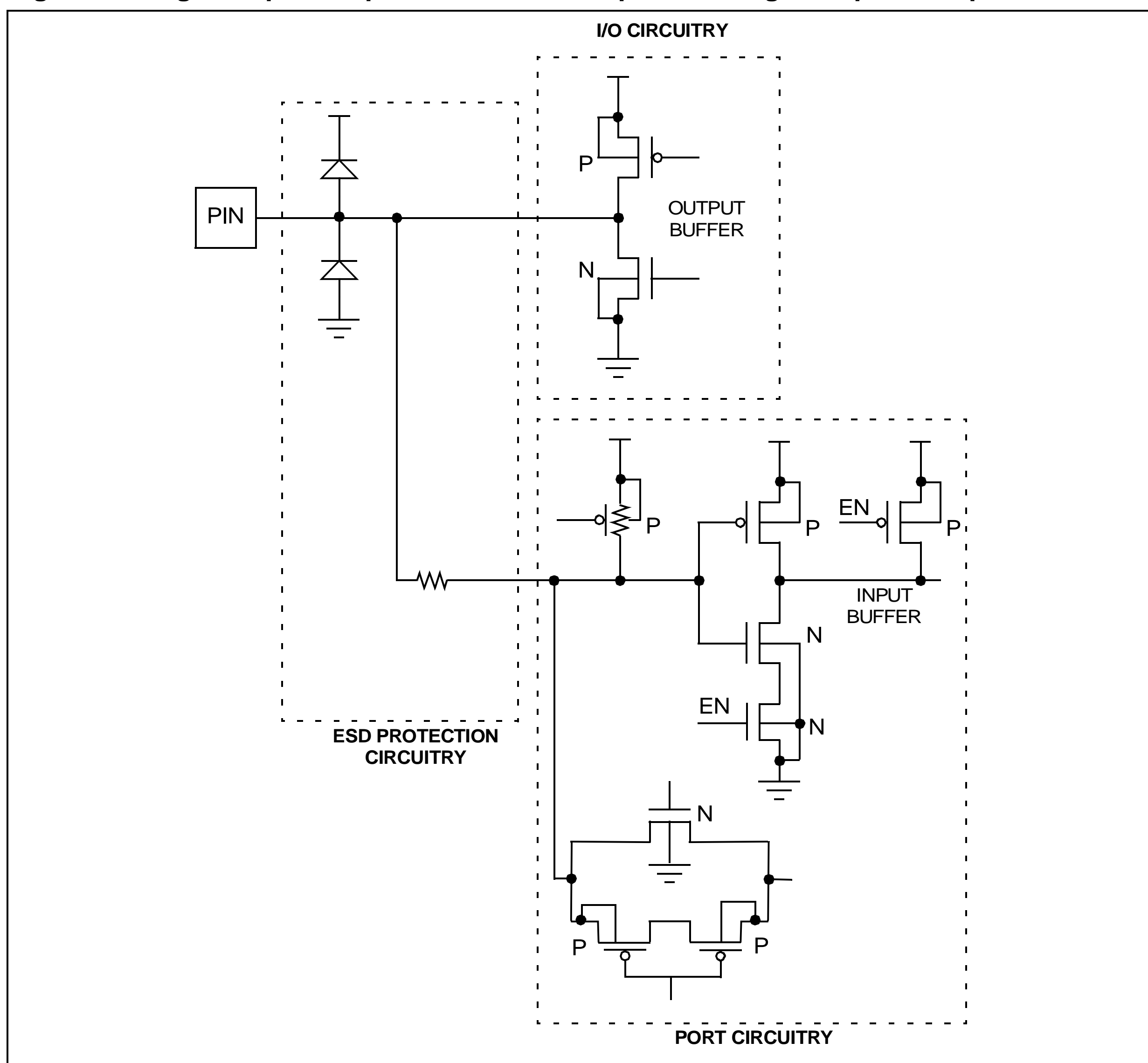
When an illegal negative voltage level is applied to the Microcontroller I/O pins (both versions, push-pull and true open-drain output) the clamp diode is always present and active (see ESD protection circuitry and N-channel driver).

3.1.3.4 Internal Circuitry: Analog Input pin

Figure 16. shows the internal circuitry used for analog input. It is primarily a digital I/O with an added analog multiplexer for the selection of the input channel of the Analog to Digital Converter (ADC).

The presence of the multiplexer P-channel and N-channel can affect the behaviour of the pin when exposed to illegal voltage conditions. These transistors are controlled by a low noise logic, biased through AV_{DD} and AV_{SS} including P-channel N-well: it is important to always verify the input voltage value with respect to both analog power supply and digital power supply, in order to avoid unintentional current injections which (if not limited) could destroy the device.

Figure 16. Digital Input/Output - Push-Pull Output - Analog Multiplexer Input



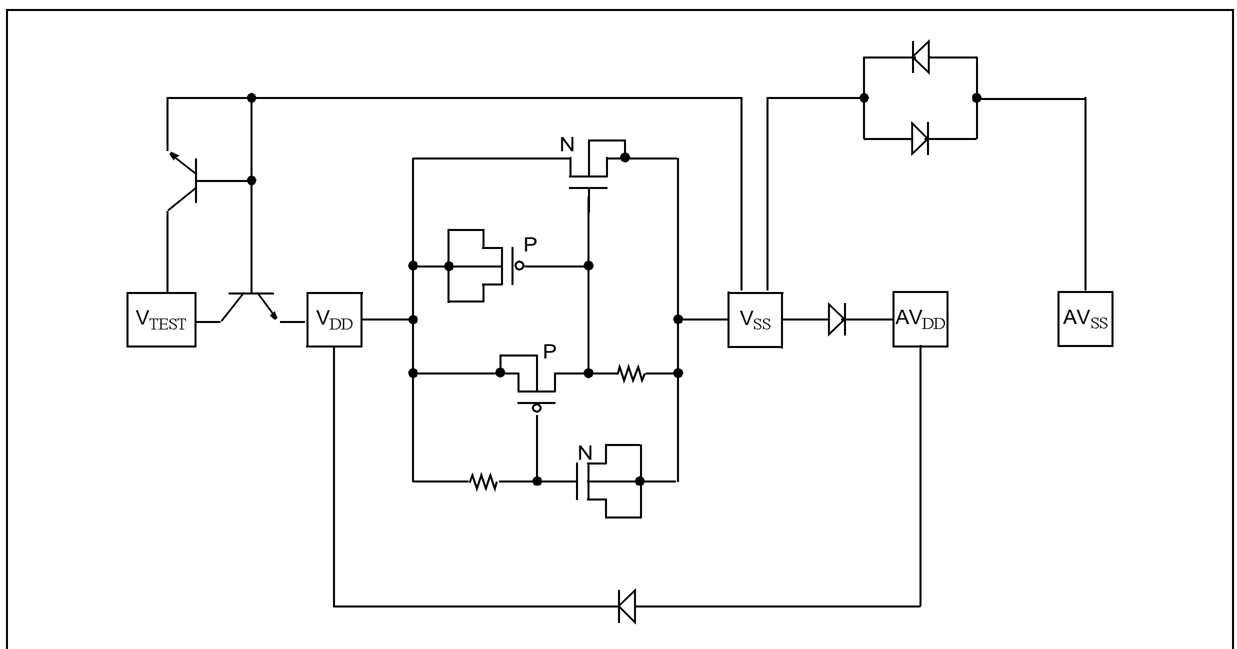
3.1.4 Multiple V_{DD} & V_{SS}.

As already said for the I/O pins, in order to ensure ST Microcontroller compliance with respect to Quality Assurance recommendations concerning ESD and Latch-up, dedicated circuits are added to the different power supply and ground pins (digital and analog). These structures create preferred paths for the high current injected during discharges, avoiding damage to active logic and circuitry. It is important for the system designer to take this added circuitry into account, when applying different current levels and voltages to the power supply and ground pins. Figure 17. shows schematically the protection net implemented on ST Microcontroller devices, composed of diodes and other special structures.

The clamp structure between the V_{DD} and V_{SS} pins is designed to be active during very fast transitions (typical of electrostatic discharges). Other paths are implemented through diodes: they limit the possibility of positively differentiating AV_{DD} and V_{DD} (i.e. $AV_{DD} > V_{DD}$); similar considerations are valid for AV_{SS} and V_{SS} due to the back-to-back diode structure implemented between the two pins. Anyway, it must be highlighted that, because V_{SS} and AV_{SS} are connected to the substrate of the silicon die (even though in different areas of the die itself), they represent the reference point from which all other voltages are measured, and it is recommended to never differentiate AV_{SS} from V_{SS}.

Note: If more than one pair of pins for V_{SS} and V_{DD} is available on the device, they are connected internally and the protection net diagram remains the same as shown in Figure 17..

Figure 17. Power Supply and Ground Configuration (on ST9)



3.2 EMISSION

3.2.1 Internal PLL

Some ST Microcontrollers have an embedded programmable PLL Clock Generator allowing the usage of standard 3 to 5 MHz crystals to obtain a large range of internal frequencies (up to 24MHz). By these means, ST Microcontroller can operate with cheaper, medium frequency crystals, while still providing a high frequency internal clock for maximum system performance. The high clock frequency source is contained inside the chip and does not go through the PCB (Printed Circuit Board) tracks and external components. This reduces the potential noise emission of the application.

The use of PLL network also filters CPU clock against external sporadic disturbances (glitches).

3.2.2 Global low power approach

3.2.2.1 Low powered oscillator

The oscillator is an major source of noise. To reduce this noise emission, the current driven by the oscillator is limited.

The main clock of some of ST Microcontrollers can be generated by four different source types coming from the multi-oscillator block (MO). This allows the designer to easily select the best trade-off in terms of cost, performance and noise emission. The clock sources are listed below in order from the most noisy to the least noisy:

- an external source
- crystal or ceramic resonator oscillators
- an internal high frequency RC oscillator

Each oscillator is optimized for a given frequency range in terms of consumption and is selectable through the option byte. The associated hardware configurations are shown in Table 11. Refer to the electrical characteristics section of the datasheet for more details in each case.

External Clock Source

In external clock mode, a clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC1 pin while the OSC2 pin is tied to ground.

Crystal/Ceramic Oscillators

This family of oscillators has the advantage of producing a very accurate rate on the main clock of the microcontroller. The selection within a list of 5 oscillators with different frequency ranges has to be done by option byte in order to reduce consumption (refer to the Microcontroller datasheet for more details on the frequency ranges). In this mode of the multi-oscillator, the resonator and the load capacitors have to be placed as close as possible to the oscillator

pins in order to minimize output distortion and start-up stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

These oscillators are not stopped during the RESET phase to avoid the delay needed for the the oscillator start-up.

Internal RC Oscillator

The internal RC oscillator is the most cost effective solution, with the drawback of lower frequency accuracy. Its frequency is in the low single digit MHz range. In this mode, the two oscillator pins have to be tied to ground.

Process variations will also bring some differences from lots to lots (20 to 60%).

Some ST Microcontrollers (refer to product specification) embed a process compensation. This feature is called “Trimmable internal RC”. A procedure during test operation analyzes the process variation and calibrate the internal oscillator accordingly. This brings the internal RC accuracy to 1%. This procedure can be also performed by the user:

Refer to AN1324 “Calibrating the RC oscillator of the ST7FLITE0 using the mains”

Table 11. ST7 Clock Sources

	Hardware Configuration		
External Clock	ST7 OSC1 OSC2 EXTERNAL SOURCE	External RC Oscillator	ST7 OSC1 OSC2 R_{EX} C_{EX}
Crystal/Ceramic Resonators	ST7 OSC1 OSC2 C_{L1} C_{L2} LOAD CAPACITORS	Internal RC Oscillator	ST7 OSC1 OSC2

The ST multi-oscillator system is designed for flexibility and to allow the system designer to find the best compromise between emission, accuracy and cost criteria.

3.2.2.2 Internal Voltage Regulators (for MCUs with low power core).

An internal Voltage Regulator is used to power some ST Microcontrollers Cores starting from the external power supply.

The Voltage Regulator reduces EMI due to the MCU Core with 2 effects:

– Lower CPU Supply Voltage

– Isolate CPU Supply from external MCU supplies.

3.2.3 Output I/O Current limitation & edge timing control

Output buffers are embedded in ST Microcontrollers, their switching speed is controlled in order to avoid parasitic oscillations when they are switched. The MCU design makes a trade-off between noise and speed.

4 EMC GUIDELINES FOR MCU BASED APPLICATIONS

The following guidelines result from experience gained in a wide variety of applications.

4.1 HARDWARE

The major noise receptors and generators are the tracks and wiring on the Printed Circuit Board (PCB), especially those near the MCU. The first actions to prevent noise problems thus concern the PCB layout and the design of the power supply.

In general, the smaller the number of components surrounding the MCU, the better the immunity versus noise. A ROMless solution, for instance, is typically more sensitive to and a bigger generator of noise than an embedded memory circuit.

Optimized PCB layout

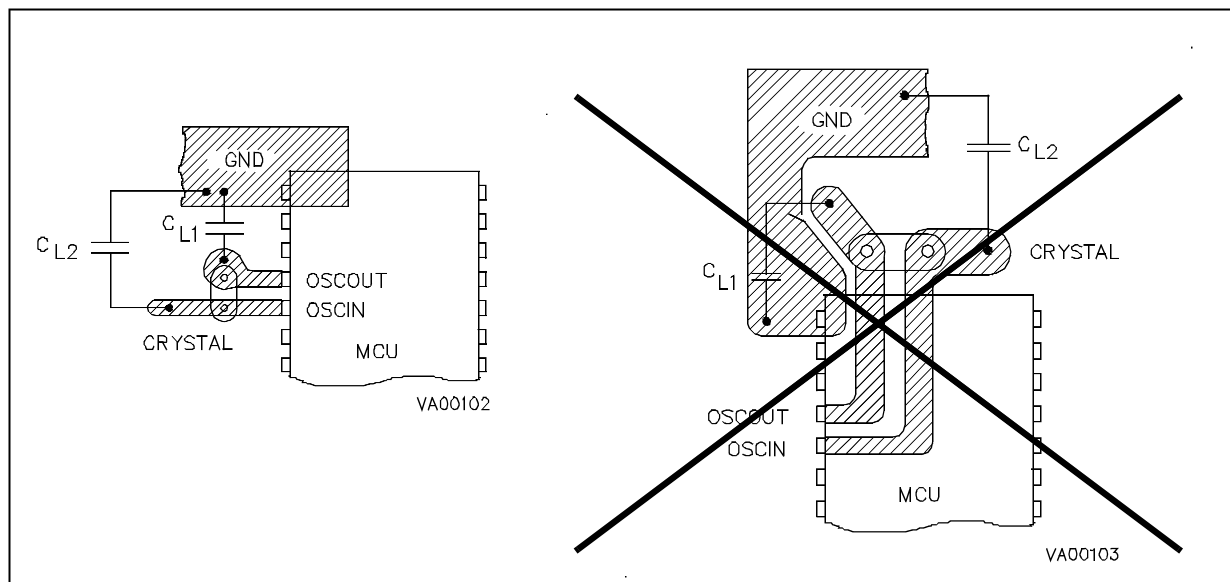
Noise is basically received and transmitted through tracks and components which, once excited, act as antennas. Each loop and track includes parasitic inductance and capacitance which radiate and absorb energy once submitted to a variation of current, voltage or electromagnetic flux.

An MCU chip itself presents high immunity to and low generation of EMI since its dimensions are small versus the wave lengths of EMI signals (typically mm versus 10's of cm for EMI signals in the GHz range). So a single chip solution with small loops and short wires reduces noise problems.

The initial action at the PCB level is to reduce the number of possible antennas. The loops and wires connected to the MCU such as supply, oscillator and I/O should be considered with a special attention. The oscillator loop has to be especially small since it operates at high frequency Figure 18.

A reduction of both the inductance and the capacitance of a track is generally difficult. Practical experience suggests that in most cases the inductance is the first parameter to be minimized.

Figure 18. PCB Board Oscillator Layout Examples



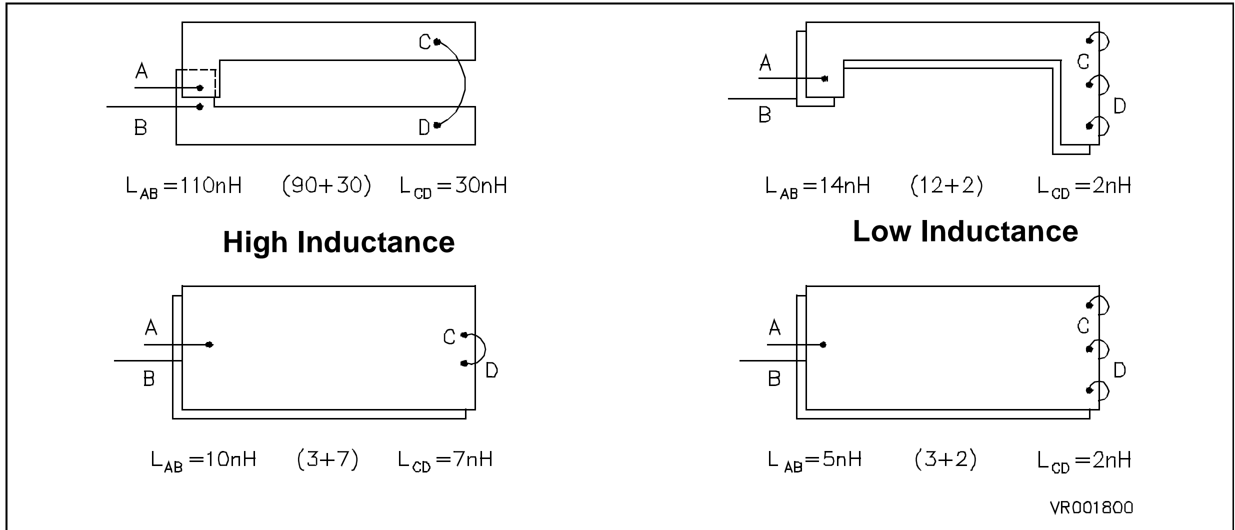
The reduction of inductance can be obtained by making the lengths and surfaces of the track smaller. This can be obtained by placing the track loops closer on the same PCB layer or on top of one another (Figure 19.). The resulting loop area is small and the electromagnetic fields reduce one another.

The ratio in order of magnitude relating to the inductance value and the area defined by the wire loop is around 10nH/cm2. Typical examples of low inductivity wires are coaxial, twisted pair cables or multiple layer PCBs with one ground and one supply layers. The current density in the track can also be smaller due to track enlargement or the paralleling of several small capacitances mounted in the current flow.

In critical cases, the distance between the MCU and the PCB, and therefore the surfaces of the loops between an MCU and its environment, has also to be minimized. This can be achieved by removing any socket between the MCU package and the PCB, by replacing a ceramic MCU package by a plastic one or by using Surface Mounting instead of Dual In Line packages.

Note: Board vias are inductances. Try to avoid them. If needed, use multi vias.

Figure 19. Reduction of PCB Tracks Loop Surfaces



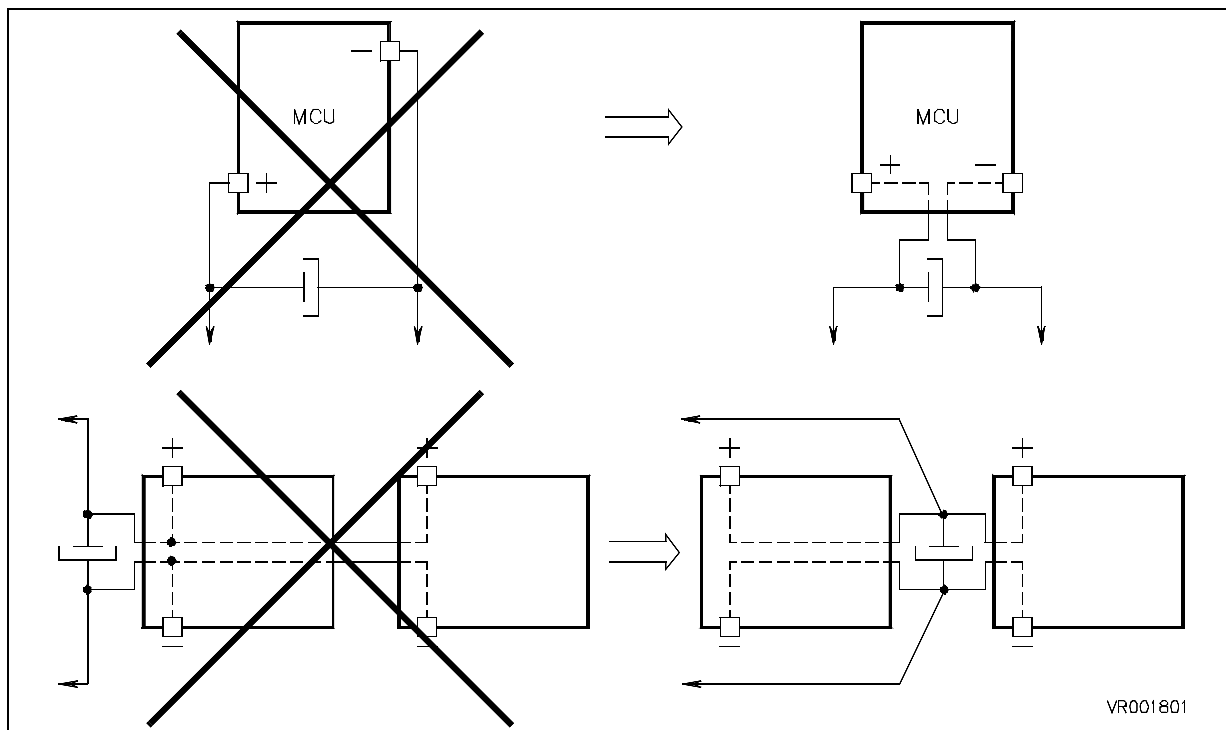
Note: This test is done with a double sided PCB. Insulator thickness is 1.5mm, copper thickness is 0.13mm. The overall board size is 65 x 200mm.

Power supply filtering

The power supply is used by all parts of the circuit, so it has to be considered with special attention. The supply loops have to be decoupled to make sure that signal levels and power currents do not interfere. These loops can be separated using star wiring with one node designated as common for the circuit (Figure 20.).

The decoupling capacitance should be placed very close to the MCU supply pins to minimize the resultant loop. It should be also large enough to absorb, without significant voltage increase, parasitic currents coming from the MCU via the input protection diodes. The decoupling of the board can be done with electrolytic capacitors (typ. 10µF to 100µF) since the dielectric used in such capacitors provides a high volumic capacitance. However these capacitors behave like inductances at high frequency (typ. above 10MHz) while ceramic or plastic capacitors keep a capacitive behaviour at higher frequency. A ceramic capacitance of, for instance, 0.1µF to 1µF should be used as high frequency supply decoupling for critical chips operating at high frequency.

Figure 20. Power Supply Lay-out Examples



I/O configuration

An open (floating) pin is a potential hazard to the circuit.

I/O pins which are not used in the application should be preferably configured in output low state. This will also minimize the current consumption.

A major source of emission in Microcontroller based applications can be due to high speed digital I/O and communication interfaces such as SPI, I2C clocks, USB or PWM... The Rise/ Fall times are critical. Typical designs add RC low pass filters.

Shielding

Shielding can help in reducing noise sensitivity and emission, but its success depends directly on the material chosen as shield (high permeability, low resistivity) and on its connection to a stable voltage source including a decoupling capacitance via a low serial impedance (low inductance, low resistance).

If the generator of major disturbances is near to the MCU board and can be identified as a strong dV/dt generator (i.e. a transformer or Klystron), the noise is carried mainly by the electrostatic field. The critical coupling between the noise generator and the control board is capacitive. A highly conductive shield (i.e. copper) creating a Faraday cage around the control board may strongly increase the immunity.

If the strongest source of perturbations is a dI/dt generator (i.e. a relay), it is a high source of electromagnetic fields. Therefore, the permeability of the shielding material (i.e. alloy) is crucial to increase the immunity of the board. In addition, the number and size of the holes on the shield should be reduced as much as possible to increase its efficiency.

In critical cases, the implantation of a ground plane below the MCU and the removal of sockets between the device and the PCB can reduce the MCU noise sensitivity. Indeed, both actions lead to a reduction of the apparent surface of loops between the MCU, its supply, its I/O and the PCB.

4.2 HANDLING PRECAUTIONS FOR ESD PROTECTION.

Electronic components have to be protected from the hazard of static electricity from the manufacturing stage down to where they are utilized in order to avoid ESD related destruction. A specific no-compromise strategy is implemented at ST for all ESD sensitive products.

From the wafer level to the shipping of finished goods, each workstation and processing step is guaranteed. For final packing, ST uses anti-static tubes. This solution ensures full ESD protection of devices. However, the supplier's greatest efforts are in vain if the end user does not provide the same level of protection and care in the application.

A relative humidity of 50% to 65% is the best to prevent electrostatic problems (the lower the relative humidity, the higher the electrostatic voltage). Nevertheless, the person handling the semiconductors as well as the equipment will be charged to a certain level. The work environment is very important to protect devices against static electricity

Anti-static electricity measures during work

(1) Conductive mat

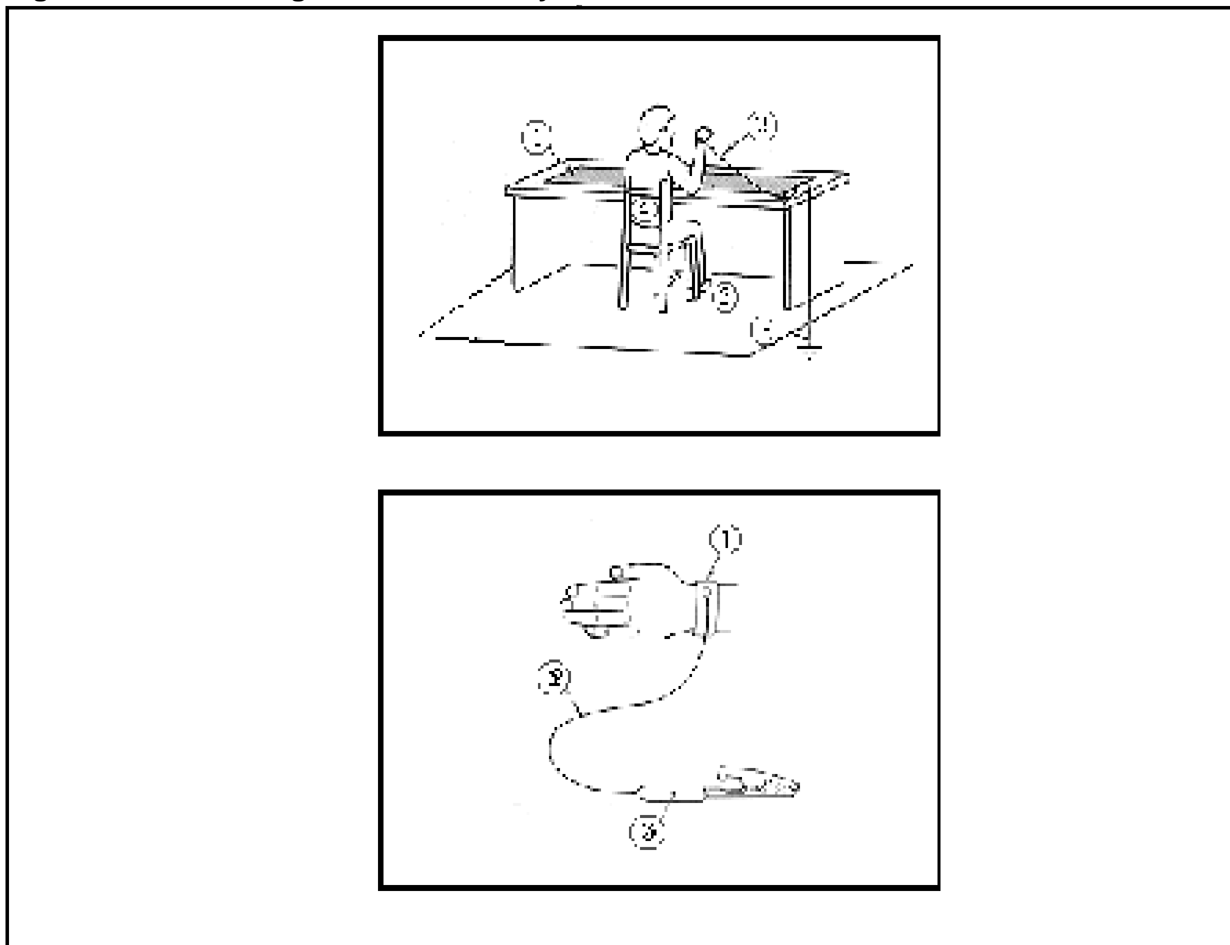
(2) Wrist

(3) Conductive floor mat

(4) Work suit with anti-static measure

(5) Conductive shoes grounding the human body

Figure 21. Grounding the Human Body



(1) Wrist ring

(2) Grounding wire: threaded copper wire, vinyl covered, about 1 meter

(3) 250 KW to 1 MW resistance is built in

Device handling:

Static control wrist straps, used and connected properly, must be worn.

All tools, persons, testing machines, which could come in contact with device leads, must be conductive and grounded. Each tabletop must be protected with a conductive mat, properly grounded. Use static control shoe strap. Use vacuum pipes.

Storage box:

Keep parts in the original packing bags up to the very last moment of the production line.

If bigger containers are used for in-plant transport of devices or PC boards, they must be electrically conductive like the carbon-loaded types. Avoid use of high dielectric materials (like polystyrene) for sub-assembly construction, storing, and transportation.

Equipment and tools:

Use Ionized air blowers to neutralize static charges of non-conductive materials.

Use only the grounded tip variety of soldering iron.

Use proper power supply systems in testing and application.

Supply voltage should be applied before and removed after input signals.

Insertion and removal of components from sockets should be carried out with no power applied.

An open (floating) pin is a potential hazard to the circuit. Each “Non Connected” pin should be grounded or connected to V_{DD} through a resistor whenever possible.

4.3 FIRMWARE

This part is Treated by a dedicated Application Note (AN1015) available on ST Website.

4.4 WEB LINKS TO EMC RELATED ORGANISATIONS

FCC: Federal Communication Commission
http://www.fcc.gov

EIA: Electronic Industries Alliance
http://www.eia.org/

SAE: Society of Automotive Engineers
http://www.sae.org

IEC: The International Electrotechnical Commission
http://wwwiec.ch

CENELEC: European Committee for Electrotechnical Standardisation
http://ww.cenelec.be

JEDEC: Joint Electron Device Engineering Council
http://www.jedec.org

5 CONCLUSION

For any microcontroller application, EMC requirements must be considered at the very beginning of the development project. Standards, features and parameters given in ST Microcontroller datasheets will help the system designer to determine the most suitable component for a given application. Hardware and firmware precautions have to be taken to optimize EMC and system stability.

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