AN2867
Application note

Oscillator design guide for STM8S, STM8A and STM32 microcontrollers

Introduction

Most designers are familiar with oscillators (Pierce-Gate topology), but few really understand how they operate, let alone how to properly design an oscillator. In practice, most designers do not even really pay attention to the oscillator design until they realize the oscillator does not operate properly (usually when it is already being produced). This should not happen. Many systems or projects are delayed in their deployment because of a crystal not working as intended. The oscillator should receive its proper amount of attention during the design phase, well before the manufacturing phase. The designer would then avoid the nightmare scenario of products being returned.

This application note introduces the Pierce oscillator basics and provides some guidelines for a good oscillator design. It also shows how to determine the different external components and provides guidelines for a good PCB for the oscillator.
This document finally contains an easy guideline to select suitable crystals and external components, and it lists some recommended crystals (HSE and LSE) for STM32 and STM8A/S microcontrollers in order to quick start development. Refer to *Table 1*for the list of applicable products.

Table 1. Applicable products

Type	Product sub-classes
Microcontrollers	STM8S Series
	STM8AF Series, STM8AL Series
	STM32 32-bit ARM Cortex MCUs

List of tables

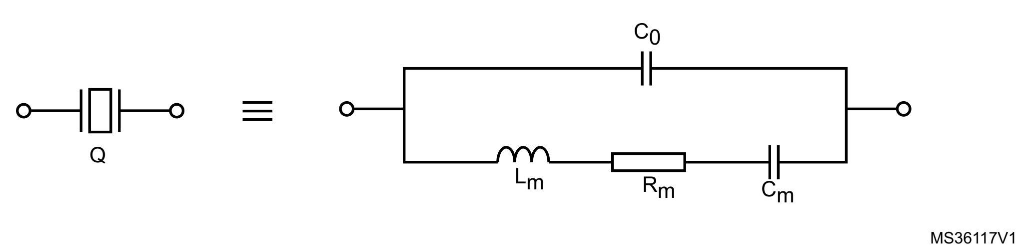
List of tables

List of figures

1 Quartz crystal properties and model

A quartz crystal is a piezoelectric device transforming electric energy to mechanical energy and vice versa. The transformation occurs at the resonant frequency. The quartz crystal can be modeled as follows:

Figure 1. Quartz crystal model



C_0: represents the shunt capacitance resulting from the capacitor formed by the electrodes

L_m: (motional inductance) represents the vibrating mass of the crystal

C_m: (motional capacitance) represents the elasticity of the crystal

R_m: (motional resistance) represents the circuit losses

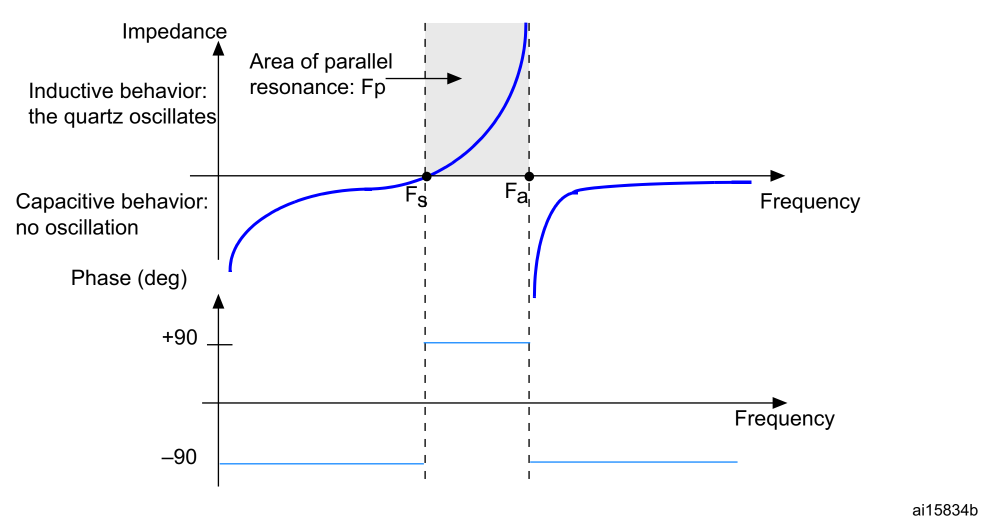
The impedance of the crystal is given by the following equation (assuming that R_m is negligible):

(1)

$$Z = \frac{j}{w} \times \frac{w^2 \times L_m \times C_m - 1}{(C_0 + C_m) - w^2 \times L_m \times C_m \times C_0}$$

Figure 2 represents the impedance in the frequency domain.

Figure 2. Impedance representation in the frequency domain



F_s is the series resonant frequency when the impedance Z = 0. Its expression can be deduced from equation (1) as follows:

(2)

$$F_s = \frac{1}{2\pi\sqrt{L_m C_m}}$$

F_a is the anti-resonant frequency when impedance Z tends to infinity. Using equation (1), it is expressed as follows:

(3)

$$F_a = F_s\sqrt{1 + \frac{C_m}{C_0}}$$

The region delimited by F_s and F_a is usually called the area of parallel resonance (shaded area in *Figure 2*). In this region, the crystal operates in parallel resonance and behaves as an inductance that adds an additional phase equal to 180 ° in the loop. Its frequency F_p (or F_L: load frequency) has the following expression:

(4)

$$F_p = F_s\left(1 + \frac{C_m}{2(C_0 + C_L)}\right)$$

From equation (4), it appears that the oscillation frequency of the crystal can be tuned by varying the load capacitor C_L. This is why in their datasheets, crystal manufacturers indicate the exact C_L required to make the crystal oscillate at the nominal frequency.

Table 2 gives an example of equivalent crystal circuit component values to have a nominal frequency of 8 MHz.

Table 2. Example of equivalent circuit parameters

Equivalent component	Value
R_m	8 Ω
L_m	14.7 mH
C_m	0.027 pF
C_0	5.57 pF

Using equations (2), (3) and (4) we can determine F_s, F_a and F_p of this crystal:

$F_s = 7988768\ \text{Hz}$ and $F_a = 8008102\ \text{Hz}$.

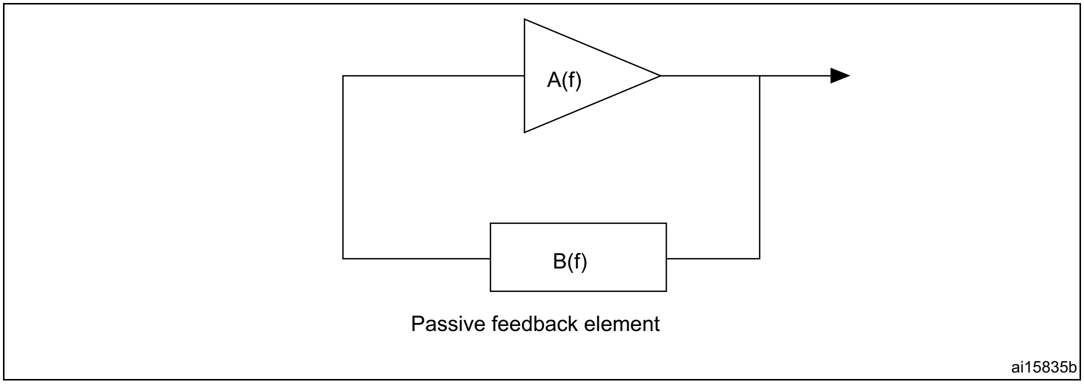
If the load capacitance C_L at the crystal electrodes is equal to 10 pF, the crystal will oscillate at the following frequency: $F_p = 7995695\ \text{Hz}$.

To have an oscillation frequency of exactly 8 MHz, C_L should be equal to 4.02 pF.

2 Oscillator theory

An oscillator consists of an amplifier and a feedback network to provide frequency selection. *Figure 3* shows the block diagram of the basic principle.

Figure 3. Oscillator principle



Where:

- A(f) is the complex transfer function of the amplifier that provides energy to keep the oscillator oscillating.

$$A(f) = |A(f)| \cdot e^{jf\alpha(f)}$$

- B(f) is the complex transfer function of the feedback that sets the oscillator frequency.

$$B(f) = |B(f)| \cdot e^{jf\beta(f)}$$

To oscillate, the following Barkhausen conditions must be fulfilled. The closed-loop gain should be greater than 1 and the total phase shift of 360 ° is to be provided:

$|A(f)| \cdot |B(f)| \geq 1$ and $\alpha(f) + \beta(f) = 2\pi$

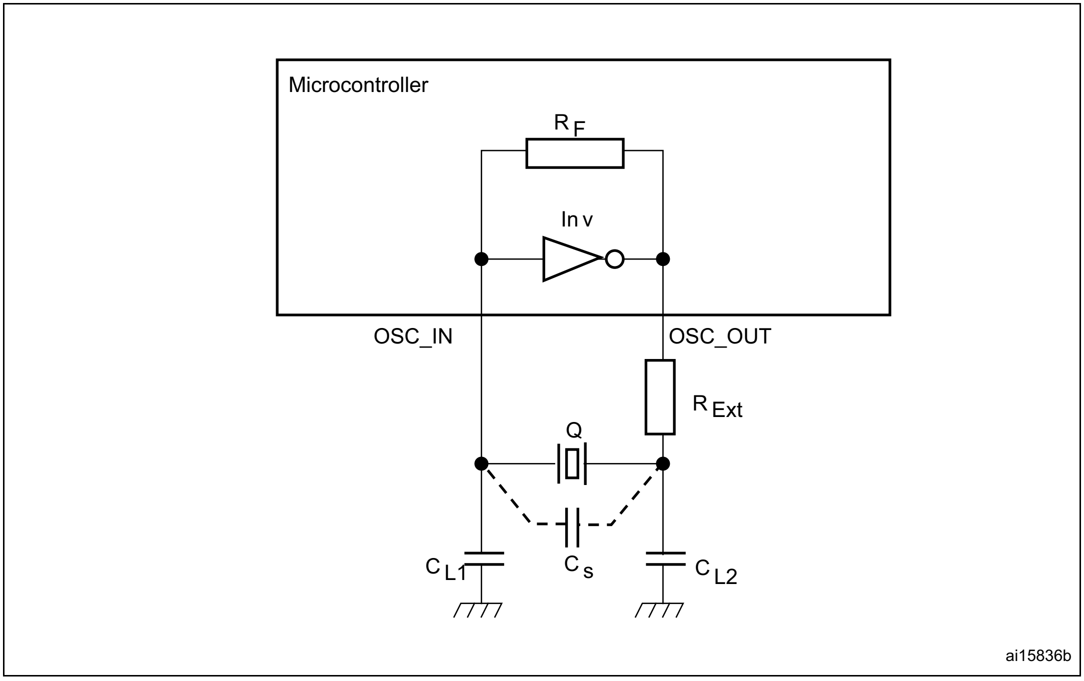
The oscillator needs initial electric energy to start up. Power-up transients and noise can supply the needed energy. However, the energy level should be high enough to trigger oscillation at the required frequency. Mathematically, this is represented by $|A(f)| \cdot |B(f)| \gg 1$ |, which means that the open-loop gain should be much higher than 1. The time required for the oscillations to become steady depends on the open-loop gain.

Meeting the oscillation conditions is not enough to explain why a crystal oscillator starts to oscillate. Under these conditions, the amplifier is very unstable, any disturbance introduced in this positive feedback loop system makes the amplifier unstable and causes oscillations to start. This may be due to power-on, a disable-to enable sequence, the thermal noise of the crystal, etc. It is also important to note that only noise within the range of serial-to parallel frequency can be amplified. This represents but a little amount of energy, which is why crystal oscillators are so long to start up.

3 Pierce oscillator

Pierce oscillators are commonly used in applications because of their low consumption, low cost and stability.

Figure 4. Pierce oscillator circuitry



Inv: the internal inverter that works as an amplifier

Q: crystal quartz or a ceramic resonator

R_F: internal feedback resistor

R_{Ext}: external resistor to limit the inverter output current

C_{L1} and C_{L2}: are the two external load capacitors

C_s: stray capacitance is the addition of the MCU pin capacitance (OSC_IN and OSC_OUT) and the PCB capacitance: it is a parasitic capacitance.

4 Pierce oscillator design

This section describes the different parameters and how to determine their values in order to be more conversant with the Pierce oscillator design.

4.1 Feedback resistor R_F

In most of the cases in ST microcontrollers, R_F is embedded in the oscillator circuitry. Its role is to make the inverter act as an amplifier. The feedback resistor is connected between V_{in} and V_{out} so as to bias the amplifier at $V_{out} = V_{in}$ and force it to operate in the linear region (shaded area in *Figure 5*). The amplifier amplifies the noise (for example, the thermal noise of the crystal) within the range of serial to parallel frequency (F_a, F_a). This noise causes the oscillations to start up. In some cases, if R_F is removed after the oscillations have stabilized, the oscillator continues to operate normally.

Figure 5. Inverter transfer function

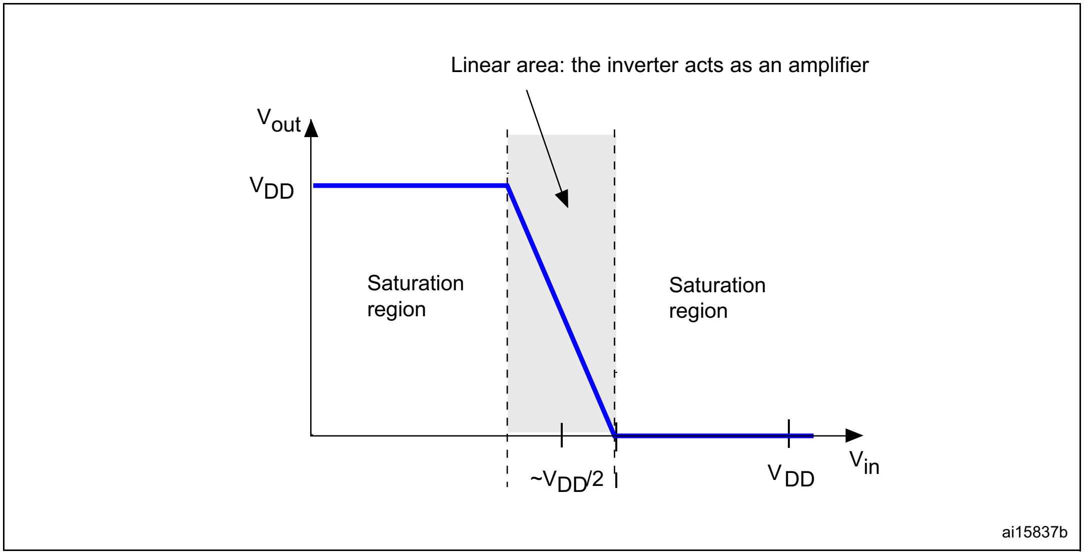


Table 3 provides typical values of R_F.

Table 3. Typical feedback resistor values for given frequencies

Frequency	Feedback resistor range
32.768 kHz	10 to 25 MΩ
1 MHz	5 to 10 MΩ
10 MHz	1 to 5 MΩ
20 MHz	470 kΩ to 5 MΩ

4.2 Load capacitor C_L

The load capacitance is the terminal capacitance of the circuit connected to the crystal oscillator. This value is determined by the external capacitors C_{L1} and C_{L2} and the stray capacitance of the printed circuit board and connections (C_s). The C_L value is specified by the crystal manufacturer. Mainly, for the frequency to be accurate, the oscillator circuit has to show the same load capacitance to the crystal as the one the crystal was adjusted for. Frequency stability mainly requires that the load capacitance be constant. The external capacitors C_{L1} and C_{L2} are used to tune the desired value of C_L to reach the value specified by the crystal manufacturer.

The following equation gives the expression of C_L:

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_s$$

Example of C_{L1} and C_{L2} calculation:

For example if the C_L value of the crystal is equal to 15 pF and, assuming that C_s = 5 pF, then:

$C_L - C_s = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} = 10\ \text{pF}$. That is: $C_{L1} = C_{L2} = 20\ \text{pF}$.

4.3 Gain margin of the oscillator

The gain margin is the key parameter that determines whether the oscillator will start up or not. It has the following expression:

$\text{gain}_{\text{margin}} = \frac{g_m}{g_{mcrit}}$, where:

- g_m is the transconductance of the inverter (in mA/V for the high-frequency part or in µA/V for the low-frequency part: 32 kHz).
- g_{mcrit} (g_m critical) depends on the crystal parameters.

  Assuming that $C_{L1} = C_{L2}$, and assuming that the crystal sees the same C_L on its pads as the value given by the crystal manufacturer, g_{mcrit} is expressed as follows:

  $g_{mcrit} = 4 \times ESR \times (2\pi F)^2 \times (C_0 + C_L)^2$, where ESR = equivalent series resistor

According to the Eric Vittoz theory: the impedance of the motional RLC equivalent circuit of a crystal is compensated by the impedance of the amplifier and the two external capacitances.

To satisfy this theory, the inverter transconductance (g_m) must have a value $g_m > g_{mcrit}$. In this case, the oscillation condition is reached. A gain margin of 5 can be considered as a minimum to ensure an efficient startup of oscillations.

For example, to design the oscillator part of a microcontroller that has a g_m value equal to 25 mA/V, we choose a quartz crystal (from Fox) that has the following characteristics: frequency = 8 MHz, C_0 = 7 pF, C_L = 10 pF, ESR = 80 Ω. Will this crystal oscillate with this microcontroller?

Let us calculate g_{mcrit}:

$$g_{mcrit} = 4 \times 80 \times (2 \times \pi \times 8 \times 10^6)^2 \times (7 \times 10^{-12} + 10 \times 10^{-12})^2 = 0{,}23\ \text{mA/V}$$

Calculating the gain margin gives:

$$\text{gain}_{\text{margin}} = \frac{g_m}{g_{mcrit}} = \frac{25}{0{,}23} = 107$$

The gain margin is very sufficient to start the oscillation and the "gain margin greater than 5" condition is reached. The crystal will oscillate normally.

If an insufficient gain margin is found (gain margin < 5) the oscillation condition is not reached and the crystal will not start up. You should then try to select a crystal with a lower ESR or/and with a lower C_L.

4.4 Drive level DL and external resistor R_{Ext} calculation

The drive level and external resistor value are closely related. They will therefore be addressed in the same section.

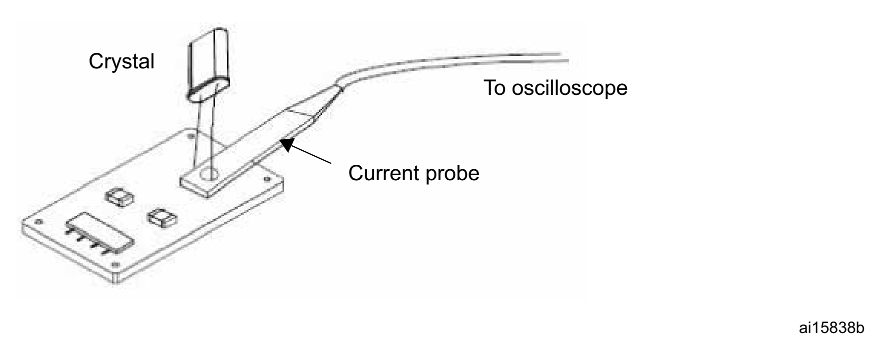
4.4.1 Calculating drive level DL

The drive level is the power dissipated in the crystal. It has to be limited otherwise the quartz crystal can fail due to excessive mechanical vibration. The maximum drive level is specified by the crystal manufacturer, usually in mW. Exceeding this maximum value may lead to the crystal being damaged.

The drive level is given by the following formula: $DL = ESR \times I_Q{}^2$, where:

- ESR is the equivalent series resistor (specified by the crystal manufacturer): $ESR = R_m \times \left(1 + \frac{C_0}{C_L}\right)^2$
- I_Q is the current flowing through the crystal in RMS. This current can be displayed on an oscilloscope as a sine wave. The current value can be read as the peak-to-peak value (I_{PP}). When using a current probe (as shown in *Figure 6*), the voltage scale of an oscilloscope may be converted into 1mA/1mV.

Figure 6. Current drive measurement with a current probe



So as described previously, when tuning the current with the potentiometer, the current through the crystal does not exceed $I_Q$max RMS (assuming that the current through the crystal is sinusoidal).

Thus $I_Q$max RMS is given by:

$$I_{Qmax}RMS = \sqrt{\frac{DL_{max}}{ESR}} = \frac{I_{Qmax}PP}{2\sqrt{2}}$$

Therefore the current through the crystal (peak-to-peak value read on the oscilloscope) should not exceed a maximum peak-to-peak current (I_{Qmax}PP) equal to:

$$I_{Qmax}PP = 2 \times \sqrt{\frac{2 \times DL_{max}}{ESR}}$$

Hence the need for an external resistor (R_{Ext}) (refer to *Section 4.4.3*) when I_Q exceeds I_{Qmax}PP. The addition of R_{Ext} then becomes mandatory and it is added to ESR in the expression of I_{Qmax}.

4.4.2 Another drive level measurement method

The drive level can be computed as:
DL= I^2_{QRMS} × ESR, where I_{QRMS} is the RMS AC current.

This current can be calculated by measuring the voltage swing at the amplifier input with a low-capacitance oscilloscope probe (no more than 1 pF). The amplifier input current is negligible with respect to the current through C_{L1}, so we can assume that the current through the crystal is equal to the current flowing through C_{L1}. Therefore the RMS voltage at this point is related to the RMS current by:

$I_{QRMS} = 2\pi F \times V_{RMS} \times C_{tot}$, with:

- F = crystal frequency
- $V_{RMS} = \frac{V_{pp}}{2\sqrt{2}}$, where: V_{pp} is the voltage peak-to-peak measured at C_{L1} level
- C_{tot} = C_{L1} + (C_s/2) + C_{probe} where:
  - C_{L1} is the external load capacitor at the amplifier input
  - C_s is the stray capacitance
  - C_{probe} is the probe capacitance)

Therefore the drive level, DL, is given by: $DL = \frac{ESR \times (\pi \times F \times C_{tot})^2 \times (V_{pp})^2}{2}$.

This DL value must not exceed the drive level specified by the crystal manufacturer.

4.4.3 Calculating external resistor R_{Ext}

The role of this resistor is to limit the drive level of the crystal. With C_{L2}, it forms a low-pass filter that forces the oscillator to start at the fundamental frequency and not at overtones (prevents the oscillator from vibrating at 3, 5, 7 etc. times the fundamental frequency). If the power dissipated in the crystal is higher than the value specified by the crystal manufacturer, the external resistor R_{Ext} becomes mandatory to avoid overdriving the crystal. If the power dissipated in the selected quartz is less than the drive level specified by the crystal manufacturer, the insertion of R_{Ext} is not recommended and its value is then 0 Ω.

An initial estimation of R_{Ext} is obtained by considering the voltage divider formed by R_{Ext}/C_{L2}. Thus, the value of R_{Ext} is equal to the reactance of C_{L2}.

Therefore: $R_{Ext} = \frac{1}{2\pi FC_2}$.

Let us put:

- oscillation frequency F = 8 MHz
- C_{L2} = 15 pF

Then: $R_{Ext} = 1326\ \Omega$

The recommended way of optimizing R_{Ext} is to first choose C_{L1} and C_{L2} as explained earlier and to connect a potentiometer in the place of R_{Ext}. The potentiometer should be initially set to be approximately equal to the capacitive reactance of C_{L2}. It should then be adjusted as required until an acceptable output and crystal drive level are obtained.

Caution: After calculating R_{Ext} it is recommended to recalculate the gain margin (refer to *Section 4.3: Gain margin of the oscillator*) to make sure that the addition of R_{Ext} has no effect on the oscillation condition. That is, the value of R_{Ext} has to be added to ESR in the expression of g_{mcrit} and $g_m \gg g_{mcrit}$ must also remain true:

$$g_m \gg g_{mcrit} = 4 \times (ESR + R_{Ext}) \times (2 \times PI \times F)^2 \times (C_0 + C_L)^2$$

Note: If R_{Ext} is too low, there is no power dissipation in the crystal. If R_{Ext} is too high, there is no oscillation: the oscillation condition is not reached.

4.5 Startup time

It is the time that take the oscillations to start and become stable. This time is longer for a quartz than for a ceramic resonator. It depends on the external components: C_{L1} and C_{L2}. The startup time also depends on the crystal frequency and decreases as the frequency rises. It also depends on the type of crystal used: quartz or ceramic resonator (the startup time for a quartz is very long compared to that of a ceramic resonator). Startup problems are usually due to the gain margin (as explained previously) linked to C_{L1} and C_{L2} being too small or too large, or to ESR being too high.

The startup times of crystals for frequencies in the MHz range are within the ms range.

The startup time of a 32 kHz crystal is within the 1 s to 5 s range.

4.6 Crystal pullability

Pullability refers to the change in frequency of a crystal in the area of usual parallel resonance. It is also a measure of its frequency change for a given change in load capacitance. A decrease in load capacitance causes an increase in frequency. Conversely, an increase in load capacitance causes a decrease in frequency. Pullability is given by the following formula:

$$\text{Pullability}_{(PPM/pF)} = \frac{C_m \times 10^6}{2 \times (C_0 + C_L)^2}$$

5 Easy guideline for the selection of suitable crystal and external components

This section gives a recommended procedure to select suitable crystal/external components. The whole procedure is divided into three main steps:

Step1: Calculate the gain margin

(please refer to *Section 4.3: Gain margin of the oscillator*)

- Choose a crystal and go to the references (chosen crystal + microcontroller datasheets)
- Calculate the oscillator gain margin and check if it greater than 5:

  If Gain margin < 5, the crystal is not suitable, choose another with a lower ESR or/and a lower C_L. Redo step 1.

  If Gain margin > 5, go to step 2.

Step2: Calculate the external load capacitors

(please refer to *Section 4.2: Load capacitor C_L*)

Calculate C_{L1} and C_{L2} and check if they match the exact capacitor value on market or not:

- If you found the exact capacitor value then the oscillator will oscillate at the exact expected frequency. You can proceed to step 3.
- If you did not find the exact value and:
  - frequency accuracy is a key issue for you, you can use a variable capacitor to obtain the exact value. Then you can proceed to step 3.
  - frequency accuracy is not critical for you, choose the nearest value found on market and go to step 3.

Step3: Calculate the drive level and external resistor

(please refer to *Section 4.4: Drive level DL and external resistor RExt calculation*)

- Compute DL and check if is greater or lower than $DL_{crystal}$:
  - If DL < $DL_{crystal}$, no need for an external resistor. Congratulations you have found a suitable crystal.
  - If DL > $DL_{crystal}$, you should calculate R_{Ext} in order to have: DL < $DL_{crystal}$. You should then recalculate the gain margin taking R_{Ext} into account.
    If you find that gain margin > 5, congratulations, you have found a suitable crystal.
    If not, then this crystal will not work and you have to choose another. Return to step 1 to run the procedure for the new crystal.

6 Some recommended crystals for STM32 microcontrollers

6.1 HSE part

6.1.1 Part numbers of recommended 8 MHz crystals

Table 4. EPSON®

Part number	ESR	C_L	C_0	Gain margin	Package
MA-406 or MA-505 or MA-506 (8 MHz)	80 Ω	10 pF	5 pF	137.4	SMD

Table 5. HOSONIC ELECTRONIC

Part number	ESR	C_L	C_0	Gain margin	Package
HC-49S-8 MHz	80 Ω	10 pF	7 pF	107	Through-hole

Table 6. CTS®

Part number	ESR	C_L	C_0	Gain margin	Package
ATS08A	60 Ω	20 pF	7 pF	56.9	Through-hole
ATS08ASM	60 Ω	20 pF	7 pF	56.9	SMD

Table 7. FOXElectronics®

Part number	ESR	C_L	C_0	Gain margin	Package
FOXSLF/080-20	80 Ω	20 pF	7 pF	43.1	Through-hole
FOXSDLF/080-20	80 Ω	20 pF	7 pF	43.1	SMD
PFXLF/080-20	80 Ω	20 pF	7 pF	43.1	SMD

6.1.2 Part numbers of recommended ceramic resonators

Table 8 gives the references of recommended CERALOCK® ceramic resonators for the STM32 microcontrollers provided and certified by Murata.

Table 8. Recommendable conditions (for consumer)

Part number	Frequency (MHz)	C_L (pF)
CSTCR4M00G55-R0	4	39
CSTCE8M00G55-R0	8	33
CSTCE8M00G15L**-R0	8 to 13.99	
CSTCE12M0G55-R0	12	
CSTCE16M0V13L**-R0	14 to 20	15
CSTCE16M0V53-R0	16	
CSTCW24M0X51R-R0	24	6

For other Murata resonators recommended for STM32 microcontrollers, please refer to *http://www.murata.com*.

6.1.3 Part numbers of recommended 25 MHz crystals (Ethernet applications)

Table 9. HOSONIC ELECTRONIC

Part number	ESR	C_L	C_0	Gain margin	Package
6FA25000F10M11	40 Ω	10pF	7pF	21.91	SMD
SA25000F10M11	40 Ω	10pF	7pF	21.91	Through-hole

Table 10. FOXElectronics®

Part number	ESR	C_L	C_0	Gain margin	Package
FOXSLF/250F-20	30 Ω	20 pF	7 pF	11.58	Through-hole
FOXSDLF/250F-20	30 Ω	20 pF	7 pF	11.58	SMD
PFXLF250F-20	30 Ω	20 pF	7 pF	11.58	SMD

Table 11. CTS®

Part number	ESR	C_L	C_0	Gain margin	Package
ATS25A	30 Ω	20 pF	7 pF	11.58	Through-hole
ATS25ASM	30 Ω	20 pF	7 pF	11.58	SMD

6.1.4 Part numbers of recommended 14.7456 MHz crystals (audio applications)

Table 12. FOXElectronics®

Part number	ESR	C_L	C_0	Gain margin	Package
FOXSLF/147-20	40 Ω	20 pF	7 pF	24.97	Through-hole
FOXSDLF/147-20	40 Ω	20 pF	7 pF	24.97	SMD

Table 13. ABRACON™

Part number	ESR	C_L	C_0	Gain margin	Package
ABMM2-14.7456 MHz	50 Ω	18 pF	7 pF	29.3	SMD

6.2 LSE part

For the low-speed external oscillator (LSE) part of STM32 microcontrollers, it is recommended to use a crystal with $C_L \leq 7$ pF.

Table 14. Recommendable crystals

Manufacturer	Quartz reference/ part number	C_L (pF)	ESR (Ohm)	Frequency (Hz)	C0 (pF)	Gm margin
Abracon	ABS07	7	70000	32768	1.05	6.5
Abracon	AB206J	6	50000	32768	1.35	10.9
Abracon	ABS25	6	50000	32768	1.35	10.9
Abracon	AB26TRB	6	50000	32768	1.35	10.9
Abracon	AB26TRJ	6	40000	32768	1.1	14.6
ACT	ACT4115A SMX	7	70000	32768	1.1	6.4
ACT	ACT3215A SMX	7	70000	32768	0.95	6.7
ACT	ACT711S	7	65000	32768	0.8	7.5
ACT	ACT201	7	50000	32768	1	9.2
ACT	ACT201	6	50000	32768	1	12.0
ACT	ACT200A	6	50000	32768	0.9	12.4
EPSON	FC135/145	7	70000	32768	1	6.6
EPSON	MC146/156	7	65000	32768	0.8	7.5
EPSON	C-002RX	6	60000	32768	0.85	10.5
EPSON	MC306/405/406	6	50000	32768	0.9	12.4
EPSON	MC30A	6	50000	32768	0.9	12.4
EPSON	C-004R	6	50000	32768	0.85	12.6
EPSON	C-005R	6	50000	32768	0.75	12.9
EPSON	C-001R	6	35000	32768	0.9	17.7
JFVNY	DT-38G06	6	30000	32768	1.3	18.44
JFVNY	MC306G06	6	50000	32768	2	9.3
KYOCERA	ST3215SB32768C0HPWBB	7	70000	32768	0.9	6.7
MicroCrystal	MS1V-T1K	6	60000	32768	0.9	10.3

7 Some recommended crystals for STM8A/S microcontrollers

7.1 Part numbers of recommended crystal oscillators

Table 15. KYOCERA

Part number	Freq.	ESR	CL	Drive level (DL)
CX5032GA08000H0QSWZZ	8 MHz	300 Ω max	12 pF	500 µW max
CX5032GA16000H0QSWZZ	16 MHz	100 Ω max	12 pF	300 µW max
CX8045GA08000H0QSWZZ	8 MHz	200 Ω max	12 pF	500 µW max
CX8045GA16000H0QSWZZ	16 MHz	50 Ω max	12 pF	300 µW max

7.2 Part numbers of recommended ceramic resonators

Table 16 and *Table 17* give the references of recommended CERALOCK® ceramic resonators for the STM8A microcontrollers provided and certified by Murata.

Table 16. Recommendable conditions (for consumer)

Part number	Freq.	CL
CSTCR4M00G55B-R0	4 MHz	$C_{L1} = C_{L2} = 39$ pF
CSTCE8M00G55A-R0	8 MHz	$C_{L1} = C_{L2} = 33$ pF
CSTCE16M0V53-R0	16 MHz	$C_{L1} = C_{L2} = 15$ pF

Table 17. Recommendable conditions (for CAN-BUS)

Part number	Freq.	CL
CSTCR4M00G15C**-R0	4 MHz	$C_{L1} = C_{L2} = 39$ pF
CSTCR8M00G15C**-R0	8 MHz	$C_{L1} = C_{L2} = 33$ pF
CSTCE16M0V13C**-R0	16 MHz	$C_{L1} = C_{L2} = 15$ pF

8 Tips for improving oscillator stability

8.1 PCB design guidelines

The 32 kHz crystal oscillator is an ultra-low-power oscillator (transconductance of a few µA/V). The low oscillator transconductance affects the output dynamics since smaller transconductance values generates a smaller oscillating current. This results in a lower peak-to-peak voltage on the oscillator outputs (from a few dozen to a few hundred mV).

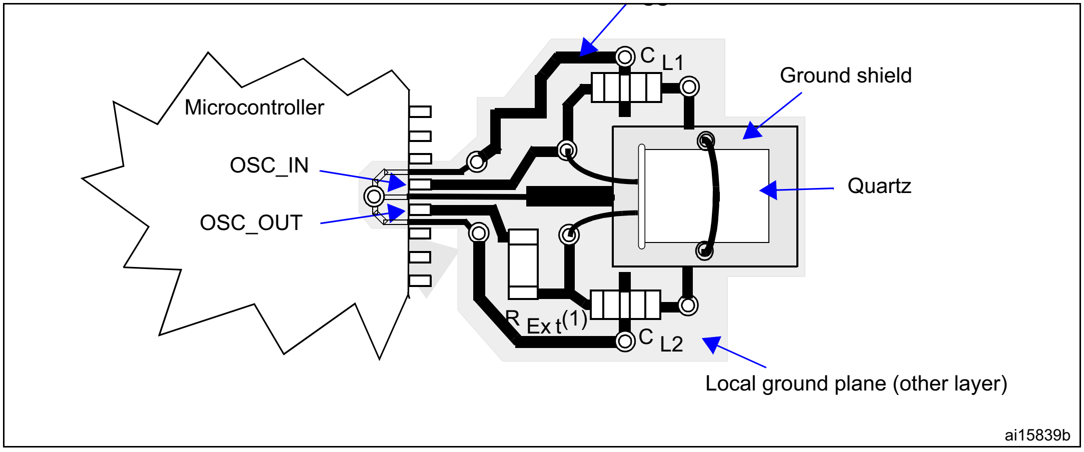
Keeping the signal-to-noise ratio (SNR) below acceptable limits for a perfect operation of the oscillator means more severe constraints on the oscillator PCB design in order to reduce its sensitivity to noise.

Therefore, great care must be taken when designing the PCB to reduce as much as possible the SNR. A non-exhaustive list of precautions that should be taken when designing the oscillator PCB is provided below:

- High values of stray capacitance and inductances should be avoided as they might lead to uncontrollable oscillation (e.g. the oscillator might resonate at overtones or harmonics frequencies). Reducing the stray capacitance also decreases startup time and improves oscillation frequency stability.
- To reduce high frequency noise propagation across the board, the MCU should have a stable power supply source to ensure noiseless crystal oscillations. This means that well-sized decoupling capacitor should be used for powering the MCU.
- The crystal should be mounted as close as possible to the microcontroller to keep short tracks and to reduce inductive and capacitive effects. A guard ring around these connections, connected to the ground, is essential to avoid capturing unwanted noise which might affect oscillation stability.

  Long tracks/paths might behave as antennas for a given frequency spectrum thus generating oscillation issues when passing EMI certification tests. Refer to *Figure 8: PCB with separated GND plane and guard ring around the oscillator* and *Figure 10: Signals around the oscillator*.
- Any path conveying high-frequency signals should be routed away from the oscillator paths and components. Refer to *Figure 8: PCB with separated GND plane and guard ring around the oscillator*.
- The oscillator PCB should be underlined with a dedicated underneath ground plane, distinct from the application PCB ground plane. The oscillator ground plane should be connected to the nearest MCU ground. It prevents interferences between the oscillator components and other application components (e.g. crosstalk between paths). Note that if a crystal in a metallic package is used, it should not been connected to the oscillator ground. Refer to *Figure 7: Recommended layout for an oscillator circuit*, *Figure 8: PCB with separated GND plane and guard ring around the oscillator* and *Figure 9: GND plane*.
- Leakage current might increase startup time and even prevent the oscillator startup. If the MCU is intended to operate in a severe environment (high moisture/humidity ratio) an external coating is recommended.

Figure 7. Recommended layout for an oscillator circuit



Warning: **It is highly recommended to apply conformal coatings to the PCB area shown in *Figure 7*, especially for the LSE quartz, CL1, CL2, and paths to the OSC_IN and OSC_OUT pads as a protection against moisture, dust, humidity, and temperature extremes that may lead to startup problems.**

8.2 PCB design examples

Example 1

Figure 8. PCB with separated GND plane and guard ring around the oscillator

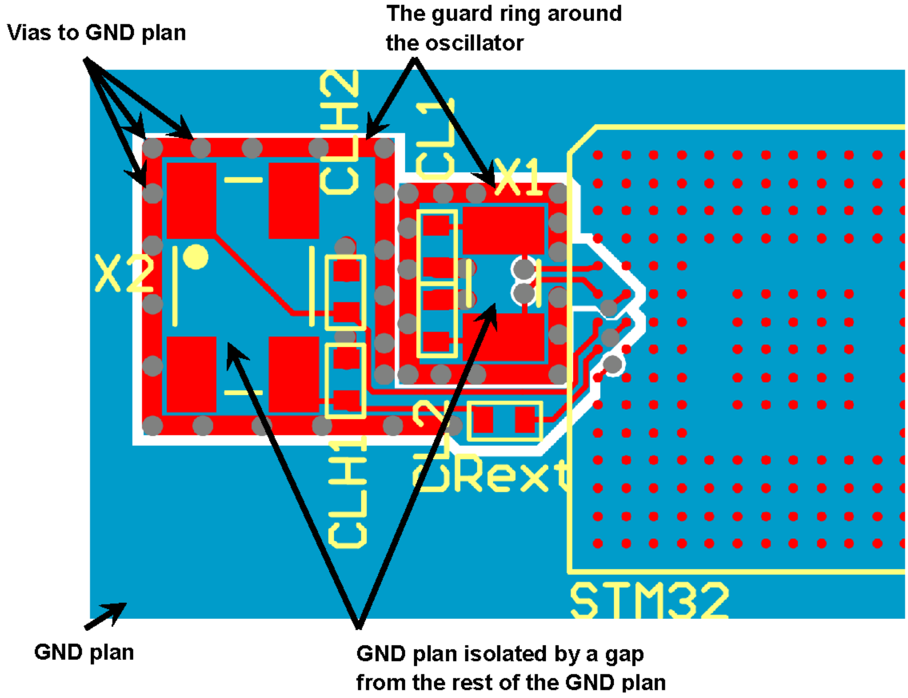
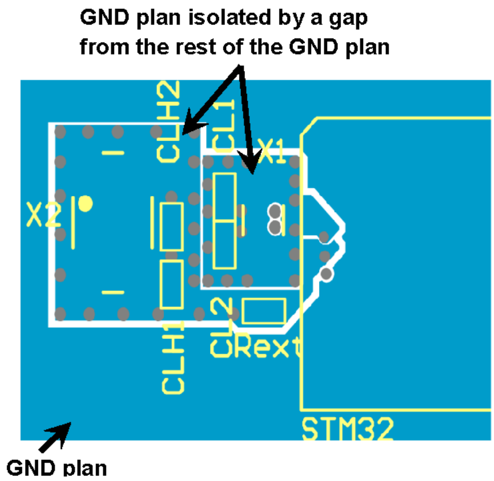
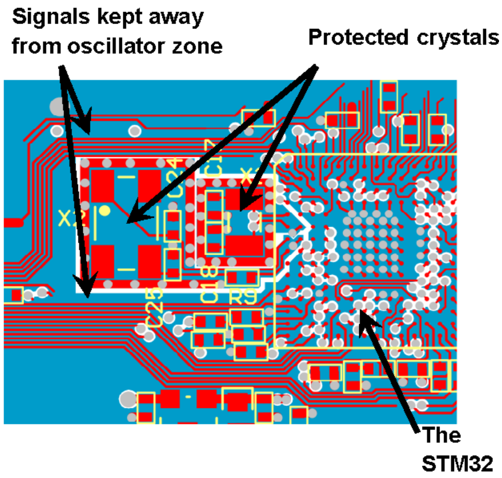


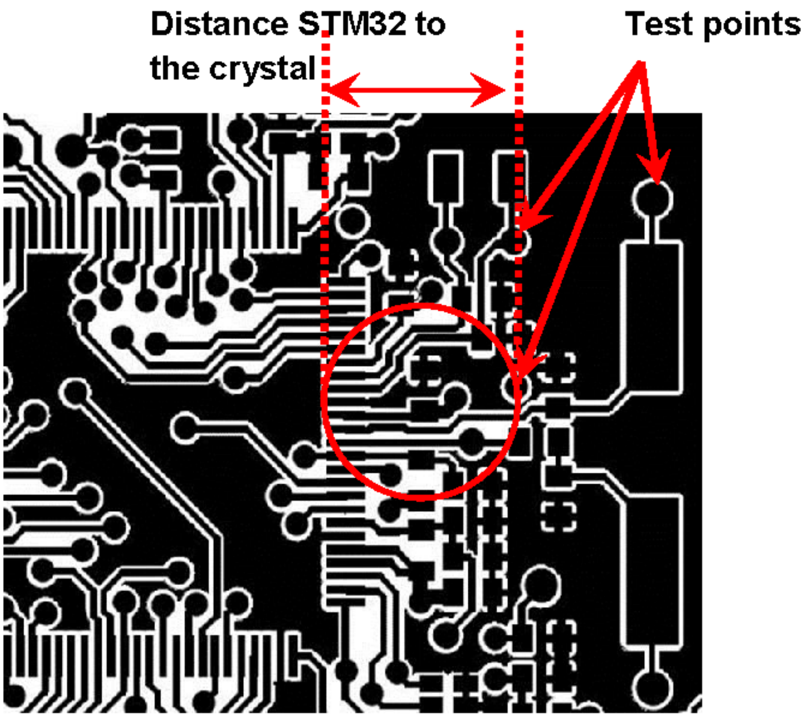
Figure 9. GND plane	Figure 10. Signals around the oscillator
	

Example 2

Figure 11 gives an example of PCB that does not respect the guidelines provided in *Section 8.1*:

- No ground plans around the oscillator component
- Too long paths
- No symmetry between oscillator capacitances
- High crosstalk/coupling between paths
- Too many test points.

Figure 11. Preliminary design (PCB design guidelines not respected)



The PCB design has been improved to respect the guidelines (see *Figure 12*):

- Guard ring connected to the GND plane around the oscillator
- Symmetry between oscillator capacitances
- Less test points
- No coupling between paths.

Figure 12. Final design (all design guidelines have been respected)

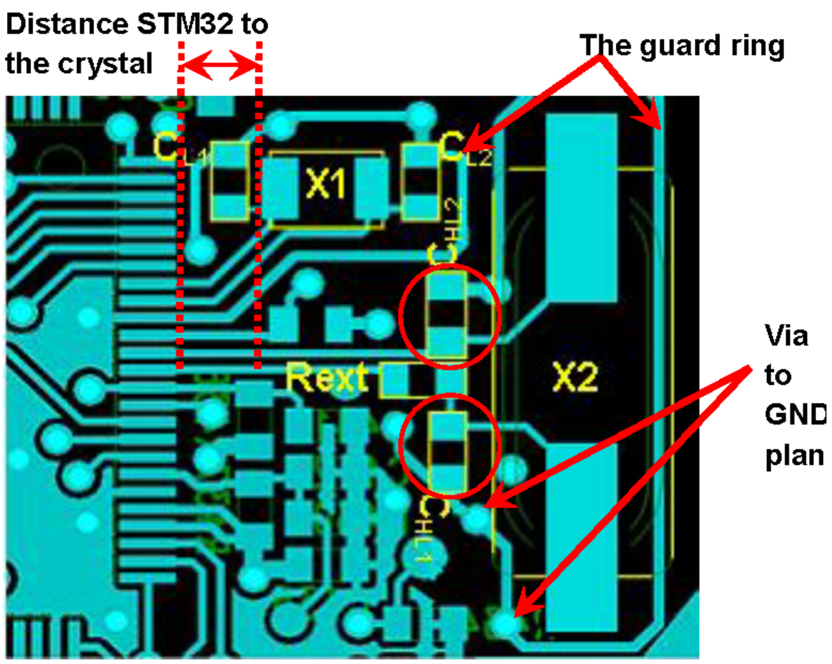
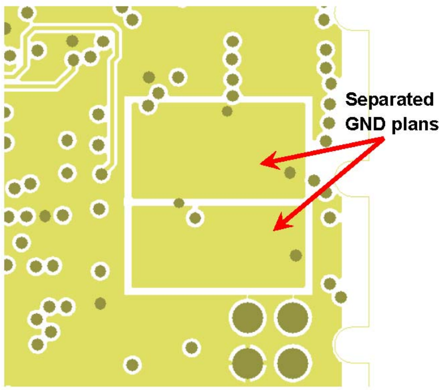
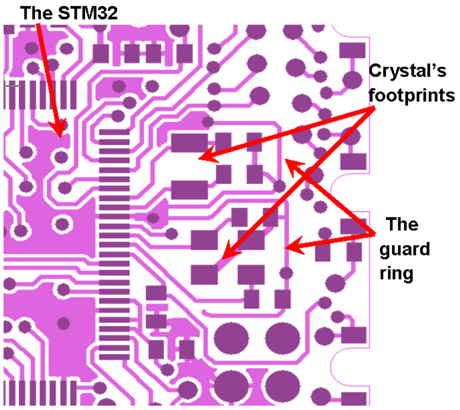


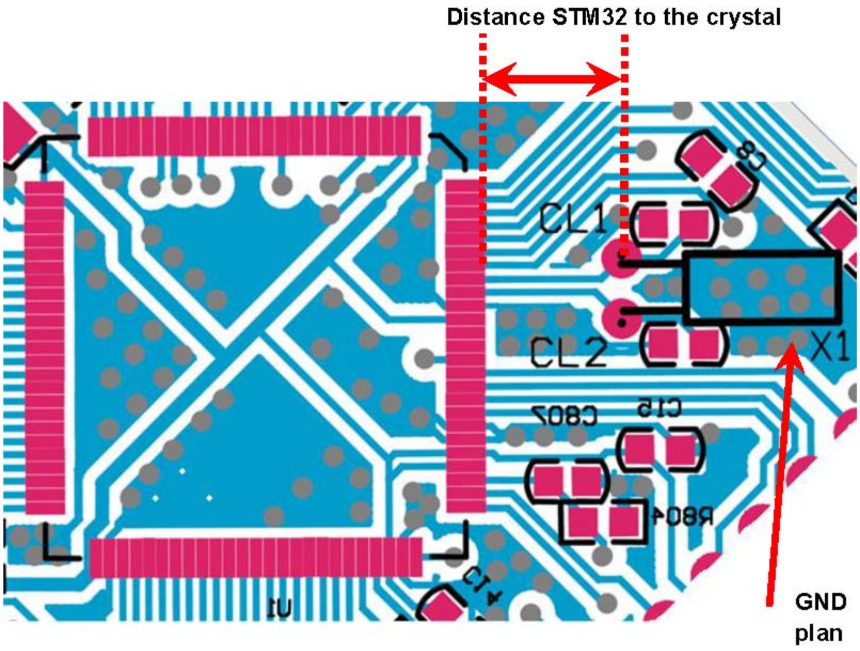
Figure 13. GND plane	Figure 14. Top layer view
 	

Example 3

Figure 15 gives another example of PCB that does not respect the guidelines provided in *Section 8.1*:

- No guard ring around oscillator components
- Long paths
- EMC tests failed.

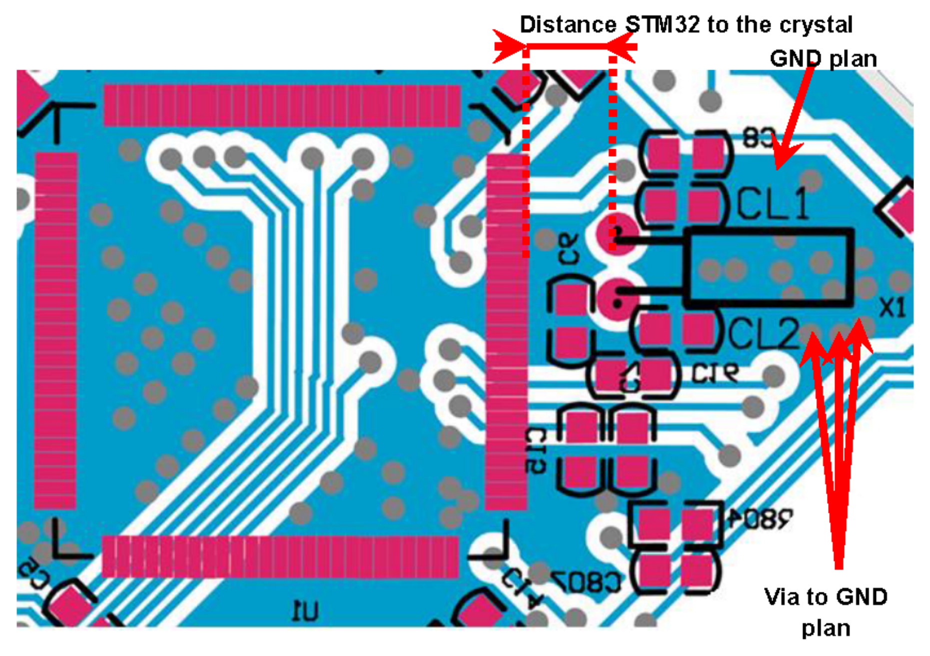
Figure 15. PCB guidelines not respected



The PCB design has been improved to respect the guidelines (see *Figure 16*):

- Ground planes around the oscillator component
- Short paths that link the STM32 to the oscillator
- Symmetry between oscillator capacitances
- EMC tests passed.

Figure 16. PCB guidelines respected



8.3 Soldering guidelines

In general, soldering is a very sensitive process for low-frequency crystals more than it is for high-frequency ones. Hints to reduce the impact of such process on the crystal parameters are provided below:

- Expose crystals to temperatures above their maximum ratings can damage the crystal and affect the ESR value. Refer to the crystal datasheet for the right reflow temperature curve. If it is not provided, ask the manufacturer.
- PCB cleaning is recommended to obtain the maximum performance by removing flux residuals from the board after assembly (even when using “no-clean” products in ultra-low-power applications).

9 Conclusion

The most important parameter is the gain margin of the oscillator, which determines if the oscillator will start up or not. This parameter has to be calculated at the beginning of the design phase to choose the suitable crystal for the application. The second parameter is the value of the external load capacitors that have to be selected in accordance with the C_L specification of the crystal (provided by the crystal manufacturer). This determines the frequency accuracy of the crystal. The third parameter is the value of the external resistor that is used to limit the drive level. In the 32 kHz oscillator part, however, it is not recommended to use an external resistor.

Because of the number of variables involved, in the experimentation phase you should use components that have exactly the same properties as those that will be used in production. Likewise, you should work with the same oscillator layout and in the same environment to avoid unexpected behavior and therefore save time.

10 Revision history

Table 18. Document revision history

Date	Revision	Changes
20-Jan-2009	1	Initial release.
10-Nov-2009	2	DL formula corrected in *Section 4.4.2: Another drive level measurement method*. Package column added to all tables in *Section 6: Some recommended crystals for STM32 microcontrollers*. Recommended part numbers updated in *Section 6.1: HSE part* and *Section 6.2: LSE part*. *Section 6.1.3: Part numbers of recommended 25 MHz crystals (Ethernet applications)* added. *Section 6.1.4: Part numbers of recommended 14.7456 MHz crystals (audio applications)* added.
27-Apr-2010	3	Added *Section 7: Some recommended crystals for STM8A/S microcontrollers*.
25-Nov-2010	4	Updated *Section 6.1.2: Part numbers of recommended ceramic resonators*: removed *Table 7: Recommendable condition (for consumer)* and *Table 8: Recommendable condition (for CAN bus)*; added *Table 8: Recommendable conditions (for consumer)*; updated Murata resonator link. Updated *Section 6.2: LSE part*: removed *Table 13: EPSON TOYOCOM*, *Table 14: JFVNY®*, and *Table 15: KDS*; Added *Table 14: Recommendable crystals*. Added *Warning:* after *Figure 7*.
30-Mar-2011	5	*Section 6.1.2: Part numbers of recommended ceramic resonators*: updated “STM32” with “STM8”. *Table 16: Recommendable conditions (for consumer)*: replaced ceramic resonator part number “CSTSE16M0G55A-R0” by “CSTCE16M0V53-R0”.
17-Jul-2012	6	Whole document restricted to STM32 devices.
19-Sep-2014	7	Changed STM32F1 into STM32 throughout the document. Added STM8AL Series in *Table 1: Applicable products* Replace STM8 by STM32 in *Section 6.1.2: Part numbers of recommended ceramic resonators* and updated hyperlink. Added *Section 8: Tips for improving oscillator stability*. Remove section *Some PCB hints*.